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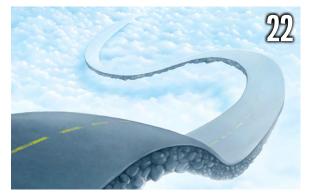
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5G: Coming to Your World Soon

We've all heard plenty about 5G lately. The transition from 3G to 4G meant a 10x increase in speed, but 5G will be at least 1,000 times faster than 4G. What does 5G mean to PCB designers and manufacturers? For this month's issue on 5G technology, we asked a variety of contributors to help us flesh it out.

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5G: It's Kind of a Big Deal

The Shaughnessy Report by Andy Shaughnessy, I-CONNECTO07

We've all had it happen: You dial a number on your cellphone, but it doesn't connect immediately. Sometimes you have to wait 10 or even 15 seconds before the other party's phone starts ringing. If you're like me, you curse at your phone, then at Verizon, and say, "They can put a man on the moon, but I have to wait 15 seconds for a phone call? This is an outrage!"

Well, help may be on the way in the form of 5G. We've all heard plenty about 5G lately. Some companies are likely to be using 5G this year, but not commercially. The first commercial 5G services probably won't be available until 2020. But behind all the hoopla, what does 5G mean to us and our industry?

The main thing to remember is that the switch from 4G to 5G is exponentially different than the move from 3G to 4G. The transition from 3G to 4G meant a 10x increase in speed; 5G will be at least 1,000 times faster than 4G. Some carriers are claiming that we'll be able to download an HD movie in less than 10 seconds. (For reference, the 3G–4G upgrade cost billions of dollars worldwide. No word on what the 4G–5G switch will cost.)

So, it's kind of a big deal. What does it mean for you and your customers?



A lot of people I've spoken with—designers, fabricators, and assembly providers—aren't sure what it's going to mean for their companies. I think it's safe to say that the majority of PCB companies are just going to wait and see how things shake out. It's difficult to build a roadmap around a technology that hasn't been implemented yet.

Many of us will be watching the 2020 Summer Olympics in Tokyo for more than cover-

age of gymnastics—NTT DOCOMO of Japan plans to launch commercial 5G services for the games. NTT DOCOMO is partnering with companies like Samsung, Huawei, Nokia, and Ericsson to have 5G up and running in two years.

Most companies working on 5G have formed alliances with other tech companies. These firms all realize that they can't implement something of this scale without strategic partnerships. Maybe our industry should try that approach more often.

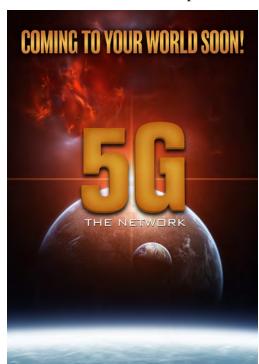
For this month's issue on

5G technology, we asked a variety of contributors to help us flesh out what this all means for PCB designers and manufacturers. In our experts discussion, John Hendricks of Rogers Corporation discusses Rogers' plans to field high-speed materials for 5G applications, and Ben Jordan of Altium explains what 5G means for EDA software tool providers. Next, Technology Editor Dan Feinberg focuses on how 5G will affect our industry, and who won't be affected by this change. CF Yee of Keysight Technologies has a feature article on PAM-4 and its application in 400-Gb Ethernet to support the huge traffic volume expected with 5G. Further, John Coonrod of Rogers discusses the challenges that 5G presents to laminate manufacturers, who will have to contend with microwave frequencies below 6 GHz and millimeter-wave frequencies of about 30 GHz.

We also have columns from regular contributors Barry Olney, Tim Haag, and Alistair Little, as well as an interview with columnist Mark Thompson and an article on constraint-driven design by Zuken's Ralf Bruening.

Speaking of Communication...

Fabricators always ask designers to communicate with them early in the design process to help avoid DFM issues later on. But is this



even possible?

Case in point: At the recent SMTA Atlanta, the Designers' Roundtable drew a group of approximately 15 designers and design engineers. Doug Philbrick of ITS, an assembly provider, and Rick Kincaid of K&F, a fabricator (who, by the way, lost about 50 pounds and looks great), were also in attendance. Doug and Rick both mentioned that they'd like to have more communication with PCB designers early in the process.

However, almost every designer in the room said

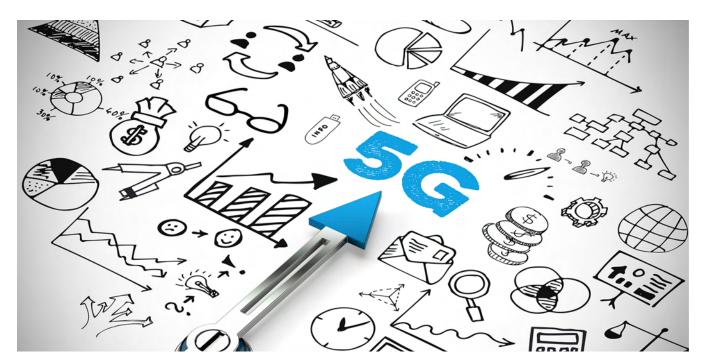
that they never knew who was going to fabricate or assemble their boards. Most designers didn't know who was going to do the protos or volume production; a few actually laughed at the idea that a designer might know who was going to turn their design into a reality.

So, is all of this preaching about talking to your fabricator early just a bunch of happy talk? I'm curious. Do you know who is going to fabricate and assemble your designs? Let me know your thoughts on this. We may be on to something.

See you next month! **DESIGN007**



Andy Shaughnessy is managing editor of *Design007 Magazine*. He has been covering PCB design for 18 years. He can be reached by clicking here.



Experts Discussion: What Does 5G Mean to Materials and EDA Tools?

Feature by the I-Connect007 Editorial Team

Whether we're ready for it or not, 5G technology is coming. While many companies are waiting to see how we're all affected by this, PCB materials providers and EDA tool vendors have no such luxury. For this issue, we spoke with John Hendricks, market segment manager for wireless infrastructure at Rogers Corporation, and Ben Jordan, director of product and persona marketing for Altium, about the challenges related to 5G and what this means for PCB designers and fabricators.

Andy Shaughnessy: John, could you tell us a little bit about what you do at Rogers and your thoughts on 5G?

John Hendricks: Rogers Corporation manufactures high-frequency printed circuit board materials. I'm a market segment manager, and that means I have responsibility for the wireless infrastructure business, globally. It's my job to identify what we need to be doing to meet both current and future needs.

And 5G has some interesting challenges. If you look at it from the PCB material point of view, in the past there was not that much change as you went from 2G to 3G to 4G. Lots of other technologies developed very dramatically of course, but in the circuit board business, not a whole lot changed in terms of what was required from materials. And the simple reason for that was that, from a hardware point of view, there were just small differences in frequencies—700 megahertz, 900 megahertz, 1.8 up to 2.5, something like that. And a power amp still basically looked like a power amp, and an antenna still looked like an antenna.

5G is interesting because, as most people know, it's split into two areas; a much bigger area, at least in the beginning, is the sub-six gigahertz market. And then you have the millimeter wave, which is 28 gigahertz. The millimeter wave presents some very dramatic changes to the material requirements because of the much higher frequency, so materials must be much lower loss. They have to be much thinner, much smoother copper.

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Down at sub-six gigahertz, there's not so much of a dramatic change in the electrical requirements of the materials, but one of the things that is happening is, perhaps not necessarily in the very first iterations, but certainly in newer designs that we see coming out on the horizon, there's a lot more integration between the antennas and the power components and the transceivers, and going forward even more integration with the high-speed digital parts.

So, you see much more complex multilayer printed circuit boards, and a lot more integration. You see these modular stacks starting to look a bit more like highspeed digital boards. And so, the manufacturability of the PCB becomes more critical, and the ability to make much complex multilayer more PCBs becomes more critical than it was from 2, 3 and 4G. I think that's how I would sum it up.

Shaughnessy: Ben, why don't

you tell us a little bit about yourself, then just give us a few thoughts on 5G.

Ben Jordan: Sure. My background is more digital than anything. I was an FPGA programmer before getting into the EDA space. For me, RF has always been this scary black box thing. And I know that 5G is going to affect many people, especially at the PCB design level. That's because those people don't necessarily have any knowledge or experience with doing RF PCB design or RF system-level design.

But the whole point of moving to 5G is to enable many thousands of additional devices to join the network, where the whole push for this from my point of view is so the Internet of Things could go to its next stage of evolution. There are going to be many thousands of devices needing reasonable bandwidth, a lot of them are going to be thirsty, and a lot of devices will have very, very small bits of information. So, if you read up on 5G, you read that there could be many hundreds of thousands of simultaneous connections from sensor arrays, or it will be used as a sensor network. Maybe the flagship consumer will still be mobile phones, but the same networks in our homes, in our streets, in our cities, are going to be 4G or 3G, will be completely saturated if all those different IoT sensors and services that we're dreaming up were to have to use those older technologies.

> That's really what's driving this and what's pushing bandwidth to be increased to accommodate this. What do vou do to increase bandwidth? You make much more complex modulation schemes, and you also must increase carrier frequency. So now with 5G we're going to be seeing in the millimeter wave, bandwidths up to 60 gigahertz, for example. What does that mean for PCB designers and people like me who don't know a lot about RF? It's kind of scary, if you

think about it.

I think, to a large extent, we have been relying on our chip manufacturers, companies like NXP or Broadcom and Qualcomm, to come up with the goods in a very easy-to-consume sort of package, so that a lot of those materials and a lot of the RF signal pathways are contained on a chip, and the antennas are there. One of the good things about high frequency carriers is the sizes of the antennas can shrink. One of the other things about 5G is its ability to go peer to peer. Then various nodes on the network will be able to quickly negotiate direct links and communicate peer to peer and not require a base station all the time.

Some of those bottlenecks will disappear and it will become more of a true mesh. And in doing so, we can have lower power requirements because there's less signal strength required in many instances. So that can help with the hundreds or thousands of sensor arrays or other smart devices. In terms of PCB design, reduc-



John Hendricks

ing power requirements can greatly simplify things. But it does increase other challenges for passing electromagnetic compatibility standards and certifications. That's going to be a huge challenge for a lot of the designers out there. And they'll have to learn more anyway, even if they're doing everything with a simple chip and a basic carrier printed circuit board, all the way to maybe a more specialized hub style device, like a tower or a node for aggregating connections.

Those boards are going to be the complex ones with exotic materials. But then hopefully the actual end-user devices will be simpler, because a lot more of the magic secret sauce will be on the chip, or in the package, or in the die. And in my mind, the problems are equally on the semiconductor companies as they are on actual board-level design engineers and PCB designers.

Shaughnessy: Right, they're supposed to start releasing commercial chips, this year and next, designed for 5G.

Jordan: I have a friend who is an RF engineer at a company that begins with Q. I was speaking with him just this morning, knowing I was going to join this discussion. And he said he's working on 5G right now, and it's very, very difficult for those guys doing the actual chip design and the analog front end. We'll see how well that goes.

Shaughnessy: One of the things that I've seen is that they're saying some of these are going to require much thicker boards. You know, they're going to demand thicker PCBs and they're going to have higher aspect ratios and it is going to be a lot harder for everybody, but harder for the fabricator to put these boards together.

John, have you seen that in your findings?

Hendricks: Yes, in truth we see a lot of people trying a lot of different solutions for the same type of problem. But there are some common threads that run through them, including a greater degree of integration that is leading

to more complex, thicker PCBs. We're talking about boards that can be 10, 14, 16, 18, or 20 layers, which we wouldn't have seen in the past on previous generations of mobile communications or what have you. So yes, you do see that complexity, and you do see much more challenge on the PCB manufacturing side, and that's what I was referring to when I was talking about the stacks starting to look like more complex high-speed digital boards than they have in the past.

Shaughnessy: As far as materials go, is it going to require a whole different set of new materials?

Hendricks: I think that depends on whether you are talking about the sub-six gigs or the millimeter wave. The sub-six gigs can broadly work with the materials that are available today. What happens at 28 gigs and higher is that you start to require, for example, extremely smooth copper. What happens in

What happens at 28 gigs and higher is that you start to require, for example, extremely smooth copper.

the millimeter wave range is that as the materials become thinner, which is simply a function of the smaller wavelength, then it's more than just having to have just a low loss dielectric. The components of insertion loss on a microstrip circuit are both conductor-based and dielectric-based, and as you get thinner the copper component of that loss becomes more important. And that's driven primarily by the smoothness of the copper, because at very high frequencies you have the skin effect and the current travels along the bottom of the copper, so things like the copper foil roughness become more important. When you start having smooth copper, that means that you have challenges with copper bond and peel strength.

With the millimeter wave, you certainly start to foresee more material challenges than you see at lower frequencies.

Jordan: I think this really does tie into the CAD side as well, because if someone doesn't have a lot of experience and knowledge, we always say, "Work with your fabricator." A lot of fab-

ricators are going to struggle with this stuff, and there will be a few leading-edge ones, and it might be more suitable for people working on 5G apps and design to work more with the materials company first than with the fabricator. I can foresee that we're going to need improved capabilities in layer stack planning, and maybe even some kind of simulation capability for things more around the mechanical limitations of laver stacks.

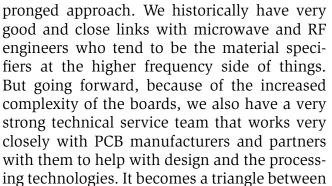
People already do thermal

analysis on their circuit board designs, they do impedance control calculations and use 2D and 3D field solvers to make sure their layer stack is going to function as desired at RF and highspeed digital edge rates. But there's going to be an increasing number of people who have a great idea but don't know the mathematics or analysis techniques behind getting something to work with an appropriate layer stack that's affordable to manufacture.

Ben Jordan

With all those tradeoffs, on the CAD side, we need to introduce capabilities in layer stack planning that will help people making those tradeoffs and reuse known good layer stacks. Maybe it would be good for us to partner with a company like Rogers and come up with sample layer stacks that people can reuse. You know, if you build it this way, specify it this way, you'll have an easier time getting your design to production.

Hendricks: Sure. At Rogers, we have a two-



the electrical designers, the manufacturers, and the material suppliers. We effectively have to work together.

Jordan: Collaboration is really the name of the game, isn't it?

Hendricks: Yup.

Patty Goldman: How often does that collaboration happen?

Hendricks: There's often this old-fashioned traditional

approach where the electrical designer designs a PCB and then goes to a PCB manufacturer and the PCB manufacturer says, "I wouldn't have designed it that way." I guess there's always an element of that in it. We don't often have three-way partners or three-way meetings, but there is a set of three-way communications. We talk closely to the PCB manufacturers and the OEMs equally, basically.

Goldman: I asked that because we hear that so often on all sorts of different subjects that "if only they could let us know first and we could all work together it would be so much better."

Hendricks: Yeah. It never goes completely smoothly (laughs).

Stephen Las Marias: Do you think these 5G challenges will have an impact on the PCB assembly side?

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Jordan: I think the issues with assembly remain the same for any kind of wireless technology. There's going to be DFT; it's going to create new problems and new opportunities, again because it's new physical connectivity and modulation schemes, and new rules from the FCC and CE and Europe and others, for making sure products don't cause problems. And all of that impacts assembly, in my mind anyway, because assembly is the first task of that final stage of production. The second half of that stage, which is done typically in the assembly process, at the end, is the test. And designing for test is going to have new challenges with 5G. I mean, how are you going to test that your devices are too chatty when it's supposed to be functioning and not using too much bandwidth on a network in a certain geographical region where there could be 1,000 other devices?

How do we test for that? And how do we design the PCB at those millimeter wave frequencies; the probe effect is going to be a huge problem. You know, the probe effect is that by measuring something you affect how it operates. So how do you measure? And that happens at those kinds of frequencies. So, the assembly houses are going to have to develop and buy new test equipment that's going to ensure these products pass muster. Not just functionally, but that they pass the rules. Maybe I have a naïve idea of that, but that's just my two cents on that question.

Las Marias: I think you're right, Ben. Thank you for that.

Shaughnessy: Happy, is there anything that we're missing? What do you think about the 5G?

Happy Holden: At Hewlett Packard, we typically would do testing for up to 800 gigahertz. When you're designing and building boards, and we have to measure something that's in 800 gigahertz, you have to be 10 times better. And so, RF design and RF materials were always a big headache, but that's where HP made a lot of money, because not too many people could build this test equipment. Now this kind of specialty, rather than being with the OEMs, is going to come down to common board fabricators and board assemblers that may not have the manpower, the equipment, the training or the knowledge. For a while there's going to be an elite few that will have mastered all these needs.

And then because of the opportunity and the prices, more people will jump in with more processes and more materials. But for the short term, this is a tough area. You know, I took a degree in electrical engineering, but because of the mathematics and field theory, I stayed away from Maxwell's equations. Unfortunately, it's coming that even digital is RF design, and you can't escape.

The only way to escape is to go optical; then you don't have to worry about it at all, because there are no magnetic fields. So, one of the alternatives may be that a lot of 5G may jump into the optical area, simply because of the inherent problems and shortages in the digital electronic area. I think that's what makes it an interesting subject. Going forward, there are an awful lot of challenges.

Shaughnessy: Right. It seems like you're just now getting to the point with millimeter wave where they can commercialize it for mainstream. I keep reading about people that have had a hell of a time with millimeter wave, but it seems like they've got it under control now.

Holden: UCLA demonstrated for us a millimeter wave chip that had only three connections, and it had replacement mechanical connectors. Because they were so directional that the transmit and receive had to be surface mounted on the edge of the PC board and you didn't need the wire or mechanical connectors because of the millimeter wavelength. A millimeter chip with its own antenna right off the die itself and they're so small you can put quite a few on a wafer. Designing and the architecture of products, they change. The follow up, we're not using mechanical connectors with sockets or anything like that anymore. **Shaughnessy:** John, is there anything you'd like to add?

Hendricks: I would just say that everything I've heard has been correct. The millimeter wave does present a lot of challenges, purely from the RF point of view, as has been pointed out. Millimeter wave is nothing new. Not even anything new in consumer applications because you'll see millions of 77-gigahertz radars being produced every year for the automotive industry now, and things like adaptive cruise control. So, from the RF point of view, it's not such a huge challenge. But people are developing new modulation technologies and all kinds of stuff that go with that, which is completely new.

From the PCB side of things, it's the complexity of the boards at those frequencies that's rather new. Even the 77-gigahertz radar is a relatively simple PCB, compared to some of the designs we are starting to see coming along in 5G.

The only other thing that I would point out is when we talk about sub-six gigahertz versus millimeter wave; it's going to be a long time before the millimeter wave really grows that quickly. The initial applications look more like fixed broadband access, and people are working on mobile applications at millimeter wave, so that is a lot more challenging. In the initial, let's say, five-year period, the vast majority of 5G designs are not going to be millimeter wave, at least in terms of production volumes. They're going to be down below six gigahertz.

Shaughnessy: Sounds like pretty interesting stuff. It sounds like it's going to make some little disruption, every step of the way. More change.

Hendricks: It's the one thing that never changes.

Shaughnessy: Well, I appreciate all of you joining us for this talk. I know you're all busy.

Jordan: You too, Andy. Thank you. DESIGN007

Tech Bends Light More Efficiently, Offers Wider Angles for Light Input

Engineering and physics researchers at North Carolina State University have developed a new technology for steering light that allows for more light input and greater efficiency. At issue are diffraction gratings, which are used to manipulate light in everything from electronic displays to fiber-optic communication technologies.

"Until now, state-of-the-art diffraction gratings configured to steer visible light to large angles have had an angular acceptance range, or bandwidth, of about 20 degrees, meaning that the light source has to be directed into the grating within an arc of 20 degrees," says Michael Escuti, a professor of electrical and computer engineering at NC State and corresponding author of a paper on the work.

"The practical effect of this - in augmented-reality displays, for example - would be that users would have a greater field of view; the experience would be more immersive," says Escuti.

The new grating achieves the advance in angular bandwidth by integrating two layers, which are superimposed in a way that allows their optical responses to work together. One layer contains molecules that are arranged at a "slant" that allows it to capture 20 degrees of angular bandwidth. The second layer is arranged at a different slant, which captures an adjacent 20 degrees of angular bandwidth.

"The next step for this work is to take the advantages of these gratings and make a new generation of augmented-reality hardware," Escuti says.





by Andy Shaughnessy I-CONNECTO07

As our consumer electronics reporter, Technology Editor Dan Feinberg has been following 5G for years, since it was a vague idea. For this issue, I asked Dan to give us a breakdown on what 5G is, what it means to our industry, and why moving from 4G to 5G is such a big deal.

Andy Shaughnessy: Our current cellular technology is 4G, so why is 5G worrying so many people in the PCB industry and electronics in general? In short, what's the big deal?

Dan Feinberg: I'm not sure if it is worrying them, but it will be a challenge for the designers. The big deal is quantum-level improvements in speed, throughput, etc. Some carriers are concerned, however, and that could cause delays. When the carriers upgraded their mobile networks from 3G to 4G some several years ago, it required many billions of dollars in investment in equipment and infrastructure. Initially, the investment did not really yield higher profits. What 4G did eventually was attract new customers, and expand the potential market.

Be aware that voice calls seem to be the best revenue stream for the carriers, and younger callers, who make up the majority of new users, seem to make fewer voice calls. They instead communicate live on iMessage or Whatsapp and a variety of other apps. Also, there is the belief that all things tech should get less costly and the newer generation believes that technology should get cheaper quickly. Therefore, there has to be some concern by the carriers that their vast sums of additional investment might not yield expected returns.

Shaughnessy: What are some of the hurdles and questions facing cellular companies who want to launch 5G networks this year?

Feinberg: There are lots of questions regarding 5G that will have to be answered, especially in the next year. First of all, what will we use the initial 5G networks for? Will it be cellular or perhaps to replace aging cable or other high-speed data transmission? Another question is



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where to initially implement, and how quickly the carrier should implement 5G. Remember, there is the issue of speed of implementation vs. cost. One more key question is also economic: Who will become a leader? Who will be one of the first to implement 5G (costly) vs. waiting, and how long should they wait before jumping in. Waiting is less costly, but there is the challenge of catching up. I think that

the hurdles and questions will become more obvious before the year end. As I often say, stay tuned!

Shaughnessy: What will 5G mean for PCB laminate suppliers? More high-speed, low-loss materials?

Feinberg: 5G will probably require better, improved circuit board laminates and conductors. I am far from an expert on this, but it seems to be obvious to some of the suppliers that the different compo-

nents for high-frequency (and perhaps many varying frequencies) circuits that will be used in a 5G network, including everything from power amplifiers to oscillators, will create new requirements and as-yet unknown issues. 5G may represent the next-gen wireless technology, but it will be a challenge to design and fabricate. I would guess that the circuit board materials used to build circuits that will operate across many different frequencies for 5G will have to undergo changes. However, it is possible that today's high-quality materials will meet some of the need.

Shaughnessy: Do you, or anyone, for that matter, know how 5G will affect PCB designers, fabricators, and assembly providers? A lot of people in the PCB world seem to have a waitand-see attitude.

Feinberg: I think that the top tier already has a good idea what they will be able to do and

what some of the initial challenges will be. They are more knowledgeable than they probably let on, and it is actually very smart to "wait and see" before going public

Shaughnessy: 5G sounds a lot like some of the speeds that our friends in RF and microwave have been dealing with for years. Will they be ahead of the 5G game?

Feinberg: I would expect so. Anyone who is used to designing and building high-speed, precision, tighter-spec devices will certainly be ahead of the game.

Shaughnessy: You've been covering CES, the Consumer Electronics Show for I-Connect007 for years. What effect do you expect 5G to have on consumer devices such as VR, AR, XR, and autonomous and electric vehicles?

Feinberg: It depends. If the XR (cross-reality) is local, such as connected to a local computer or network, with no wireless, 5G will not be a factor. But if it is across the network (Internet) there will be much higher capability, lower lag, and higher resolution. For global XR such as sports events, remote medical treatment, remote military ops, gaming across the net and for greatly improved resolution and response, 5G will be a hugely positive factor, in my opinion. I strongly feel that humanity has entered the "If you can imagine it, it can be done" era, and 5G will be a big enabler to making this happen.

Shaughnessy: Thanks for the insight, Dan.

Feinberg: Thank you, Andy. DESIGN007



Dan Feinberg

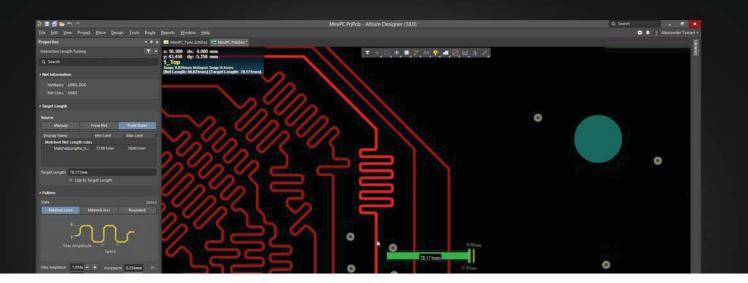


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by Chang Fei Yee KEYSIGHT TECHNOLOGIES

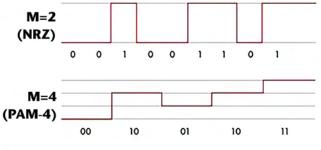
This article briefly introduces the 4-level pulse amplitude modulation (PAM-4) and its application in 400 Gigabit Ethernet (400GbE), to support the booming data traffic volume in conjunction with the deployment of 5G mobile communications. Furthermore, this article also highlights the essential pre-layout effort from signal integrity perspective for physical (PHY) link design on printed circuit board (PCB), including material selection, transmission line design and channel simulation to support 56Gbps data rate that paves the way for seamless communication in 400GbE.

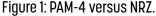
Introduction

400GbE is a new wired communication standard to accommodate the booming data traffic volume with the implementation of 5G mobile communications ^[1]. In the implementation of 400GbE communication, electrical interface with 4-level pulse amplitude modula-

tion (PAM-4) signaling over 8 lanes is adopted. The communication of eight lanes at 56Gbps (i.e., 28GBaud) per lane enables the total bandwidth of 400Gbps over the ethernet. The electrical specifications of 400GbE with PAM-4 signaling are defined in IEEE 802.3bs ^[2].

PAM-4 has 4 digital amplitude levels, as shown in Figure 1^[3]. It has an advantage over non-return-to-zero (NRZ) signals because each level or symbol in PAM-4 contains two information bits providing twice as much data throughput for the same baud rate. For instance, 28GBaud is equivalent to 56Gbps in PAM-4 and 28Gbps in NRZ respectively ^{[3] [4]}.





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Essential pre-layout effort from signal integrity perspective

According to guidelines, a PAM-4 channel with trace length up to 8 inches on a PCB shall have insertion loss less than 10dB at 14GHz (i.e., Nyquist frequency of 28GBaud) and 20dB at 28GHz (i.e., 2nd harmonic of 28GBaud) respectively ^[2] to achieve seamless data communication between the transceivers. Eight essential pre-layout efforts from signal integrity perspective to be discussed in the following:

A. Substrate material selection

There are three types of PCB substrate dielectric materials categorized based on the dielectric property (e.g., loss tangent and dielectric constant). As seen in Table 1, high-loss materials (e.g., Nelco N4000-6) have a loss tangent above 0.02 and dielectric constant above 4; medium-loss material (e.g., Isola FR408) has a loss tangent of about 0.01 and dielectric constant between 3 and 4. Meanwhile, low-loss materials (e.g., Isola I-Tera MT40) have a loss tangent of about 0.003 and dielectric constant 3.45 ^[5]. Dielectric attenuation is directly proportional to the loss tangent and square root of dielectric constant, as shown in Equation 1 ^[6].

(Equation 1)

Dielectic attenuation = 0.91 * f * loss tangent * $\sqrt{\varepsilon_r}$ dB/cm

 ε_{r} = dielectric constant

f = frequency in GHz

Simulated plot of differential insertion loss for dielectric loss effect of 8-inch differential

Materials	Dielectric constant	Loss tangent	Example
High-loss	4.3	0.023	Nelco N4000-6
Medium- loss	3.6	0.01	Isola FR408
Low-loss	3.45	0.003	Isola I-Tera MT40

Table 1: Categories of dielectric materials.

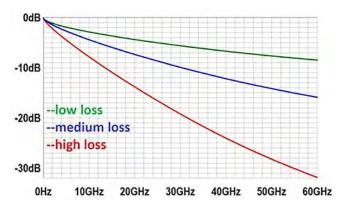


Figure 2: Simulated plot of differential insertion loss for dielectric loss effect with Hyperlynx.

microstrip signals in Figure 2 quantifies the dielectric attenuation for high, medium and low loss materials as 10dB, 5.5dB and 3.5dB respectively at 14GHz. Referring to the guide-line mentioned earlier (i.e., insertion loss less than 10dB at 14GHz for trace length up to 8 inches), low loss material shall be selected to allow more headroom contributed by other channel losses.

B. Fiber weaving

PCB dielectric substrate is composed of woven fiber-glass bound together with epoxy resin. The microscopic top view of PCB substrates of fiber weave styles 1080 and 3313 are illustrated in Figure 3^[7]. A higher number of fiber glass style (e.g., 3313), refers to denser fiber glass weaving.

Fiber glass material has dielectric properties that differ very much from the properties of epoxy resin. For instance, NE-glass fiber has dielectric constant (Dk) and loss tangent (Df) 4.4 and 0.0006 respectively ^[8]. Meanwhile epoxy resin has Dk 3.2 ^[8], which is lower than

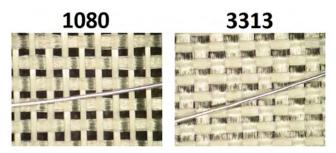


Figure 3: Fiber weave with glass style 1080 versus 3313.

fiber glass. When a substrate of sparse fiber weaving is used, PCB traces could cross different regions of resin and fiber glass more frequently. As a result, the speed or propagation delay of the signal changes frequently along the trace from transmitting to receiving end. The relationship between them is governed by Equation 2^[9].

$$v = \frac{c}{\sqrt{D_k}}$$

Where:

v = signal's speed on PCB (in unit inch/ns) c = speed of light (~12 inches/ns) D_v = dielectric constant

This scenario poses a great challenge to multi-gigabit differential signals. The homogeneous substrate is the most desired ideal condition, where substrate segment of noninverting signal has the same dielectric properties as inverting signal. However, practically, depending on the fiber weave density, nonhomogeneous substrate condition (i.e., when non-inverting signal is routed on fiber glass, while inverting signal crosses resin region or vice versa) is encountered. Due to the changing propagation delay experienced by the inverting signal, the phase difference between non-inverting and inverting signals in common mode could be much less than 180 degrees at the receiving end. The large extent of skew or misalignment between the rising and falling edges leads to the reduction of width and height of the eye diagram, equivalent to larger differential insertion loss. Ultimately, high bit error is experienced.

Figure 4 depicts the simulated plot of differential insertion loss for fiber weave effect on differential microstrip signals 8 inches in length. When the non-homogeneous substrate segment increases from 5% to 20% of total channel length, the channel attenuation is increased in the range of 0.7dB and 4dB versus 100% homogeneous at 14GHz. Hence, substrate with denser fiber weave such as 3313 shall be used.

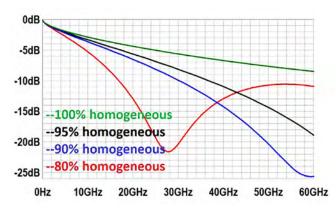
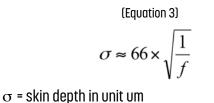


Figure 4: Simulated plot of differential insertion loss for fiber weave effect with Hyperlynx.

C. Copper surface roughness

Surface roughness of the copper for trace routing promotes its adhesion to the substrate during PCB fabrication. However, it is necessary to keep the roughness magnitude small. This is because the current of the signal tends to propagate more closely to the surface of the copper trace when the frequency of the signal gets higher. Skin depth is the parameter that determines how extensive the current of signal travels with reference to the surface of the transmission channel. The relationship between skin depth and the signal frequency is governed by Equation 3^[10].



f = frequency of signal in unit MHz

There are mainly two types of copper foil used for PCB fabrication, namely rolled copper and electrodeposited (ED) copper. Each type of copper foil has many variations that come with different typical surface roughness. For example, rolled annealed copper has roughness 0.3 um while high profile ED copper has roughness 2.2 um ^[11]. At a given skin depth, a larger magnitude of roughness causes more resistance to the signal propagation.

Figure 5 depicts the simulated plot of differential insertion loss for conductor surface



Figure 5: Simulated plot of differential insertion loss for copper surface roughness effect with Hyperlynx.

roughness effect on a microstrip channel eight inches in length. At 14GHz, 0.3um roughness introduces an additional 0.5dB, while 1.8 um roughness adding an extra 2.5dB attenuation versus a totally smooth copper surface. Hence, hardware developer shall choose the PCB fab houses that offer copper foil type with surface roughness 0.3 um or less to mitigate the attenuation and distortion of the signal transmission.

D. Minimizing via stub

Blind or back-drilled vias (Figure 6) shall be applied for IC pin break out on PCB to minimize the stub length, which in turn pushes the quarter wave resonant frequency higher, thereby increasing the bandwidth of the physical channel. With reference to Equa-

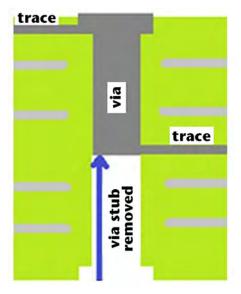
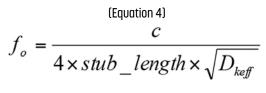


Figure 6: Blind or back-drilled via.

tion 4 ^[12], the quarter wave resonant frequency is inversely proportional to the stub length. Rearranging Equations 4 and 5 ^[13], for 56Gbps (i.e., 28GBaud) PAM-4 transmission on PCB with low-loss material, where Dkeff is 3.45, the maximum stub length would be ~ 11 mils.





 $f_o > 2 \ge 2 \ge 5 \ge 100$ x 2.5 x baud rate

Where:

f_a = quarter wave resonant frequency (Hz)

c = speed of light (~12 inches/nano-second) stub_length in inches

D_{koff} = effective dielectric constant

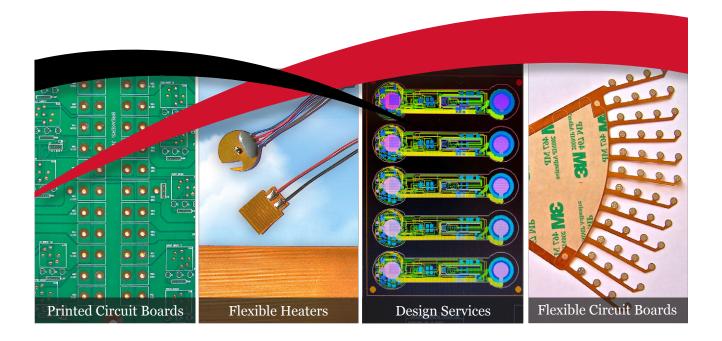
E. Minimizing impedance mismatch due to mounting pad of AC coupling capacitor

The mounting pad of the AC coupling capacitor has wider copper versus the PCB trace. For example, the capacitor in a 0201 package has 10 mil pad width, while 0603 package has 30 mil pad width ^[14], while PCB microstrip trace width is normally set not more than 10 mils. Referring to Equation 6 and 7 respectively ^[15], a wider copper in mounting pad versus PCB trace increases the capacitance, which in turn causes capacitive discontinuity or mismatch to the characteristic impedance of the transmission line in single ended mode.

Figure 7 depicts the simulated plots of differential insertion loss for microstrip traces (i.e., 500 mil long and 6 mil wide in singleended mode) interface with capacitor in 0201, 0402 and 0603 package respectively. A wider mounting pad contributes to a larger impedance discontinuity, which in turn causes a larger insertion loss due to more severe signal reflection. The attenuation at 14GHz due to 0603 (i.e., 1.2dB) and 0402 (i.e., 0.4dB) packages are at least double of 0201 (i.e., 0.2dB). Hence, designers should use capacitors in a



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smaller package, e.g., 0201 (i.e., 10 mil pad width) to minimize the discontinuity.

(Equation 6)

$$Z_o = 31.6 \times \sqrt{\frac{L_o}{C_o}}$$

Where:

- L_o= intrinsic loop inductance per unit length of the transmission line (in nH/cm)
- C₀= intrinsic capacitance per unit length of the transmission line (in pF/cm)
- Z_o = characteristic impedance (in ohm)

(Equation 7)

$$C = \frac{\varepsilon_r \varepsilon_o wl}{d}$$

Where:

- C = capacitance (in pF)
- ϵ_r = relative permittivity of substrate
- ε_0^{1} = permittivity of vacuum
- w = width of SMT pad (in cm)
- I = length of SMT pad (in cm)
- d = distance between mounting pad and reference plane underneath (in cm)

F. Providing continuous reference plane

When the PCB trace crosses over a gap between 2 split planes, an inductive impedance discontinuity or non-continuous refer-

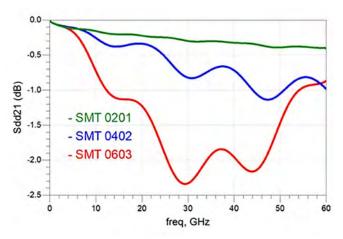


Figure 7: Differential insertion loss for varying surface mount pad width in series with 500 mil long PCB trace, simulated in Keysight EMPro. ence is encountered. This phenomenon is governed by Equations 6 and 8 ^[15] respectively. When the gap between split planes is crossed over, the distance between the trace and reference underneath (i.e., gap depth) is increased, this leads to the rise of inductance, which in turn causes the trace impedance to increase over the split. With reference to simulated plots of differential insertion loss in Figure 8, where crossing over split planes results in higher insertion loss due to larger inductive impedance discontinuity, with minimum 0.1dB attenuation at 20GHz and beyond.

(Equation 8)

$$L \approx 2x [\ln(\frac{5.98d}{0.8w+t})]$$

Where:

- L = parasitic inductance of copper trace (in nH)
- d = distance between copper trace and reference underneath (cm)
- w = width of copper trace (cm)
- t = thickness of copper trace (cm)
- x = length of copper trace (cm)

In addition to that, non-continuous reference plane or return path also creates larger loop areas that increase mutual inductance and signal crosstalk ^[16]. Hence, it is essential to ensure a solid reference plane along the entire trace length path.

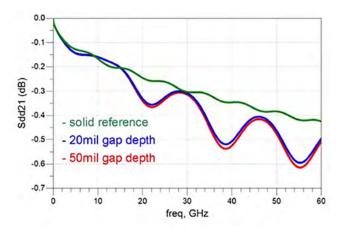


Figure 8: Differential insertion loss for 500 mil PCB trace with solid reference versus crossing over split planes simulated in Keysight EMPro.

G. Minimizing signal crosstalk

Crosstalk causes noise induction in victim signals which in turn increases the bit error at receiving IC. Therefore, in addition to providing continuous reference plane mentioned above, non-interleaved routing shall also be applied on stripline, due to a lower far end crosstalk (FEXT) compared to near end crosstalk (NEXT). Whereas interleaved routing be applied on microstrip due to a lower NEXT compared to FEXT. Channel analysis ^[17] compares the NEXT versus FEXT on microstrip and stripline respectively in time domain. Besides that, inter-pair spacing shall be at least triple the trace width ^[18].

H. Intra-pair skew

Intra-pair skew in PCB traces introduces higher insertion loss, which in turn increases the bit error of the physical channel, due to the fact that when inverting and non-inverting signals are not 180 degrees out of phase, the eye height in differential mode becomes smaller. The impact of intra-pair skew on signal integrity is shown in differential insertion loss plots in Figure 9, where larger skew leads to higher insertion loss. Therefore, each physical channel's intra-pair skew shall be kept within 5mil to mitigate the transmission loss. The skew

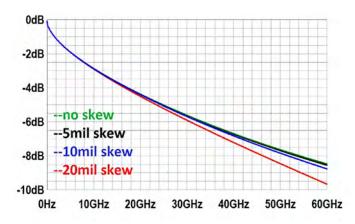


Figure 9: Differential insertion loss plots for eight-inch PCB trace with varying intra-pair skew simulated in Hyperlynx.

can be minimized using serpentine routing technique ^[19]. However, the differential impedance changes once the intra-pair spacing is increased in serpentine segment. Hence, intrapair spacing for serpentine and non-serpentine segments shall not differ too much, to minimize the full path differential impedance tolerance or discontinuity within $\pm 5\%$.

PAM-4 channel simulation

Figure 10 depicts the channel simulation topology using Keysight ADS at BER 1e-6, where

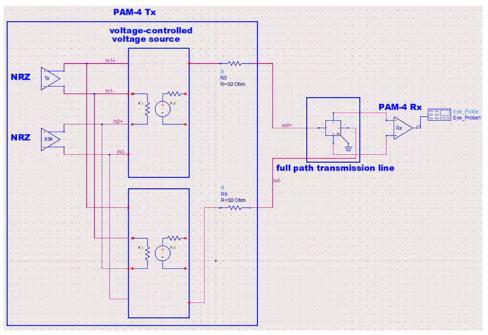


Figure 10: PAM-4 channel simulation topology at 28GBaud using Keysight ADS.

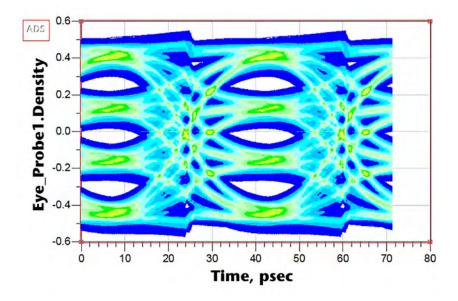


Figure 11: Eye diagram at receiver resulted from channel simulation topology in Figure 10.

two NRZ signals at 28GBaud are injected to voltage-controlled voltage source to generate a PAM-4 signal at 56Gbps. Simulation models of PCB traces, break out vias, transmitter IC package and receiver IC package are lumped in the full path transmission line. At the transmitting end, the signal amplitude and rise/fall time are 1.2Vpp and 16ps respectively. The PAM-4 eye diagram in Figure 11 has three eyes due to its four digital amplitude levels. Decision feedback equalization (DFE) at receiver is enabled. The channel simulation yields 90mV eve height and 15ps eve width. The results have to meet the specification in ^[20] before PCB prototyping for actual physical layer compliance test in ^[21].

Conclusion

All the essential pre-layout effort discussed in this article should be taken seriously in designing PAM-4 PHY channels on PCB, including material selection, transmission line design and channel simulation. It is important to implement the 56Gbps PAM-4 PHY link in a stringent manner to guarantee a robust and seamless communication between the highspeed transceivers, paving the way for reliable 400GbE. **DESIGN007**

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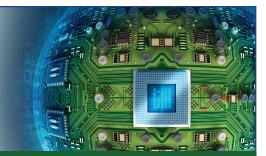
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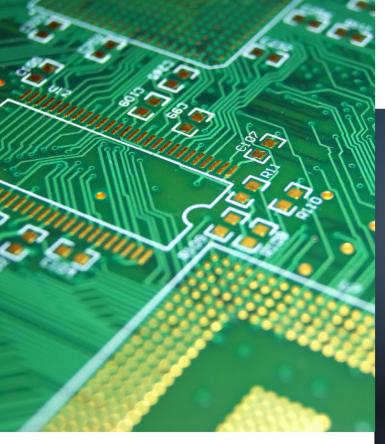
Making the Most of PCB Materials for 5G Microwave and mmWave Amps

by John Coonrod Rogers Corporation

Millions of cellphones trying to connect voices and download unimaginable numbers of files worldwide point to the inevitability of fifth generation (5G) wireless communications networks. 5G is coming, and it will require the right circuit materials for many different types of high-frequency circuits, including power amplifiers (PAs). 5G represents the latest and greatest in wireless technology, and it will be challenging to design and fabricate, starting with the circuit board materials, because it will operate across many different frequencies, such as 6 GHz and below, as well as at millimeter-wave frequencies (typically 30 GHz and above). It will also combine network access from terrestrial base stations and orbiting satellites. But by careful consideration of mechanical and electrical requirements, high-frequency circuit materials can be specified that enable the design and development of 5G PAs no matter the frequency.

Ideally, a single circuit material would be a suitable starting point for PAs at all frequencies. However, amplifiers at different frequencies have different design requirements and are best supported by circuit materials with different characteristics best suited to the different frequencies. For example, insertion loss or dissipation factor can be more or less depending on the type of circuit material. Every circuit material will suffer some amount of loss, which typically increases with increasing frequency. The loss performance of a given circuit material may be acceptable within the microwave frequencies to be used in 5G networks but not within the millimeter-wave frequency range, where signal power tends to be less with increasing frequencies. The circuit material that provides the low loss needed for high PA gain and output power at microwave frequencies may not be the best choice of material for a PA at millimeter-wave frequencies.

The design requirements for a key circuit material parameter, dielectric constant (Dk), are much different for microwave frequencies,







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such as the 6 GHz and below used with 5G systems, than for millimeter-wave frequencies, such as 30 GHz and above, as will be used for short-range backhaul links in 5G wireless networks. Selecting an optimum circuit material for each band of frequencies requires understanding which Dk value best supports each of the two different frequency ranges. Then it is a matter of finding circuit materials that possess those Dk values along with as many as possible of the other circuit material attributes that help make a good, high-performance, high-frequency PA.

Selecting an optimum circuit material for each band of frequencies requires understanding which Dk value best supports each of the two different frequency ranges.

Whether for microwave or millimeter-wave frequencies, circuit materials for high-frequency PAs must be capable of supporting circuitry that achieves the impedance match to the power transistors in those PAs. Such impedance matching is also necessary for the active devices in lower-power amplifiers, such as driver amplifiers and even in low-noise amplifiers (LNAs).

Suitable circuit materials for such impedance-matching networks must be capable of keeping circuit impedance variations to a minimum, and this is typically done through tight control of the substrate thickness, with no variations in thickness; tight control of conductor widths, such as microstrip transmission lines, to maintain the same impedance; tight control of the copper thickness on circuit laminates; and tight control of the circuit material's Dk, especially with temperature. Although using a circuit material with tight control of Dk, such as 3.50 ± 0.05 , can help maintain the impedance of high-frequency transmission lines within a narrow window as might be needed for impedance matching within a PA circuitry, variations in the substrate thickness can have even more impact on maintaining consistent impedance of high-frequency transmission lines. A circuit material with a Dk tolerance of ± 0.05 or lower is considered to have a tightly controlled Dk value.

With increasing frequencies, signal wavelengths are decreasing, requiring ever-smaller circuit features. Many of the PA circuit configurations used at both microwave and millimeterwave frequencies, such as Doherty amplifiers, are dependent upon quarter-wavelength transmission-line circuit structures and the dimensions of these structures are a function of the substrate thickness. If that circuit substrate thickness is not tightly controlled, it is easy to understand how the impedance of extremely fine transmission-line and circuit structures can vary with those variations in substrate thickness. In general, a substrate thickness variation of $\pm 10\%$ or better is a sign of tightly controlled circuit material thickness.

Feeling the Heat

Whether at microwave or at millimeter-wave frequencies, PA circuits are subject to performance variations brought about by changes in temperature, from both the operating environment and from the PA's own active devices, such as power transistors or ICs. In the search for circuit materials for both microwave and millimeter-wave PAs for 5G applications, finding circuit materials capable of effective thermal management is critical to minimizing a PA's performance variations as a result of the thermal rise brought about by its own active devices. Two circuit material parameters are of particular interest when assessing a material's thermal behavior: thermal conductivity and thermal coefficient of dielectric constant (TCDk).

High thermal conductivity allows for efficient flow of heat away from any heat-generating active devices mounted on a PCB, such as a PA's power transistors. Consistent heat flow not only removes the heat as a threat to the reliability of the transistors, but helps minimize thermally inducted PA performance variations. Thermal conductivity of 0.5 W/mK or higher is considered good for a PCB material.

TCDk is a circuit material parameter that indicates how that material's Dk is affected by variations in temperature. Ideally, a material would have a TCDk of 0 ppm/°C for no change in Dk with temperature. But practical circuit materials exhibit some changes in Dk with temperature and a TCDk of 50 ppm/°C is considered good for a circuit material, resulting in only small changes in Dk with temperature. For the amplifiers and other circuits in 5G systems that will rely on fine quarter-wavelength circuit structures, circuit materials with low TCDk values will help minimize performance variations.

The smaller wavelengths and circuit features needed for millimeter-wave PAs and circuits in general will require thinner substrate materials compared to lower-frequency microwave PAs and circuits, and maintaining a tight tolerance in that thickness is just as critical as for thicker materials. Those thinner circuit materials can also be more sensitive than thicker circuit materials to the effects of other circuit material characteristics, such as copper surface roughness. Copper surface roughness can result in such circuit effects as transmission-line loss and phase variations, so copper surface roughness should be minimized in any circuit materials specified for the smaller-wavelength, higherfrequency circuits in both 5G microwave and millimeter-wave PAs.

As an example, Rogers offers a variety of materials with different thicknesses and other characteristics needed for the two different frequency ranges. For 5G PAs at 6 GHz and below, 20- and 30-mil-thick ceramic-based RO4385 circuit laminates are low-cost circuit materials that maintain consistent performance across wide temperature ranges. They have a Dk of 3.48 in the z-axis at 10 GHz, tightly controlled within ± 0.05 . They are ideal for competitive applications and can be fabricated with standard epoxy/glass (FR-4) processes.

For 5G PAs at millimeter-wave frequencies, 5- and 10-mil-thick RO3003 laminates consist of PTFE with ceramic filler. They feature a Dk of 3.0 in the z-axis at 10 GHz tightly controlled within \pm 0.04. They feature extremely low loss at higher frequencies that helps get the most gain from the active devices in an amplifier circuit, even at the various millimeter-wave bands expected to serve the many backhaul links of future 5G wireless networks. **DESIGN007**

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Design for Magnetoelectric Device May Improve Your Memory

For years, manufacturers have offered computers with increasing amounts of memory packed into smaller devices. But semiconductor companies can't reduce the size of memory components as quickly as they used to, and current designs are not energy-efficient. One promising version of magnetic device relies on the magnetoelectric effect. Existing devices, however, tend to require large magnetic and electric fields that are difficult to produce and contain.

One potential solution for this problem is a new switch-

ing element made from chromia (Cr2O3), which, one day, may be used in computer memory and flash drives. "The device has better potential for scaling, so it could be made smaller, and would use less energy once it's suitably refined," said Randall Victora, a researcher at the University of Minnesota and an author on the paper.

Next, Victora and Ahmed aim to collaborate with colleagues who work with chromia to build and test the device. If successfully fabricated, then the new device could potentially replace dynamic RAM in computers.



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It's Only Common Sense: Taming the Extraordinary Salesperson >

We spend a great deal of time talking about how to handle poor-performing salespeople those who are not making their numbers, or those who just can't seem to get out there and visit customers, get an appointment, or close a sale.

IPC 6012-DA Revisions: The Approach to Cleanliness, Thickness, Inspection, and Wicking ►

IPC's Automotive Addendum task group was started in November 2014 and the first edition of IPC 6012-DA was released in April 2016. We are now working on the revised version and expect a release in Q2 2018. As standards need to evolve, develop and follow the needs of the industry, this work is continuous.

PCB Manufacturing (R)evolution in the Making >

At the recent HKPCA and IPC Show 2017 in Shenzhen, China, I was able to interview Les Sainsbury, CEO, and Andrew Kelley, CTO, of XACT PCB, as well as Alex Stepinski, vice president of Whelen Engineering's PCB Fab Business Unit, to discuss process evolution and technology developments in the PCB manufacturing industry.

Flex to Divest Multek's China Operations to MFLEX >

Flex Ltd. has entered into an agreement with Multi-Fineline Electronix Inc. (MFLEX), a wholly-owned subsidiary of Suzhou Dongshan Precision Manufacturing Co., Ltd (DSBJ), to divest the China-based operations of the Flex subsidiary, Multek.

Weiner's World–March 2018 🕨

SEMICON China 2018 was amazing in its size and attendance. More than 1,000 exhibitors filled an event venue of more than 74,000 square meters of exhibition space—the size of nearly 10 professional soccer fields. This year's theme was "collect, collaborate, innovate."

Aspocomp Acquires Technopolis Facility in Finland

Aspocomp Group Plc has acquired the production facility from Technopolis Plc, located in the Linnanmaa district in Oulu, Finland.

IPC APEX EXPO 2018..the Show Goes On! >

Access I-Connect007's first edition of *Show & Tell Magazine* as a flip book! Inside you will find exclusive interviews, photos, videos, contest results, and commentary that will show and tell you all about this year's event.

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Common Symptoms of Common-Mode Radiation

Beyond Design

by Barry Oiney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Electromagnetic radiation from digital circuits, can occur as either differential mode or common mode. Differential mode is typically equal and opposite and therefore any radi-

ating fields will cancel. Conversely, common-mode radiation from two coupled conductors is identical. It does not cancel but rather reinforces.

Unfortunately, differentialmode propagation can be converted to common mode by parasitic capacitance or any imbalance caused by signal skew, rise/fall time mismatch or asymmetry in the

channel. Also, return path discontinuities can create large common mode loop areas that increase series inductance and electromagnetic radiation. In this month's column, I will explore the common symptoms of, and present some cures for, common mode radiation.

Differential mode radiation accompanies normal circuit operation and is the result of current flowing in the return path loop formed by the PCB conductors (traces and reference planes, as in Figure 1). Microstrip (outer layer) loops can act as small antennae that predominately radiate magnetic fields, whereas stripline (inner layer) loops only emit radiation from the fringing fields at the edge of the PCB. Although these signal loops are necessary for circuit operation, their size and loop area must be controlled during the design process to minimize radiation.

> Fortunately, it is not necessary to evaluate each loop individually. However, the most critical loops should be

analyzed. The other loops can be controlled by good stackup design practices. Please refer to the structural guidelines in my *Beyond Design: Stackup Planning Parts 1-4* columns ^[1] for further information.

Generally, the most critical loops are the highest frequency where the signal is periodic. In a synchronous circuit, the clock is a sequence of repetitive pulses that generates the most emis-

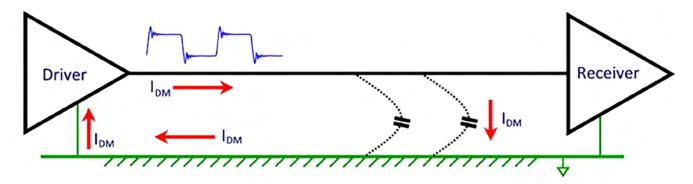


Figure 1: Normal (differential mode) signal return current.



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sions. Clock signals should always be routed first, and every effort should be made to route them in the absolute minimum loop area possible. The length of the clock trace should be minimized as well as the number of layer transition vias. On a multilayer PCB, clocks should be routed on a stripline (inner layer) adjacent to a solid reference plane to reduce radiation. The spacing between the clock trace and the return plane should be as small as possible to increase coupling and reduce loop area. Also, to prevent the clocks from coupling to cables, that leave the PCB assembly, the clock circuitry should be located well away from I/O connectors and cables.

Data and address buses, together with their associated command and control signals, are second on the critical list. These buses are normally terminated and can carry large peak currents that radiate proportionally to the current transferred. Transient power supply currents can be another significant source of differential radiation. Although these loops can be quite small, they can carry large currents during switching.

Differential mode radiation is proportional to the frequency squared and can be controlled by reducing the power distribution network (PDN) impedance to below the required target impedance, minimizing the loop area, cancelling out the fields by using differential signals and by dithering the clocks. If the amplitude of the emission is spread out, in the frequency band, then the radiation is also reduced. Spread spectrum clocking can reduce the radiation by up to 15dB.

If a differential pair is well balanced, then tight coupling will achieve an effective degree of field cancellation. However, if they are not perfectly balanced (Figure 2), then the degree of cancellation is not determined by the spacing, but rather by the common mode balance of the differential pair. Most digital drivers have poor common mode balance and therefore differential pairs often radiate far more power in the common mode than in the differential mode. In such a case, one gains no radiation benefit from coupling the differential traces more closely together. Figure 3 highlights the simulated common-mode return current in the reference plane of the cross-section of an imbalanced differential pair.

Differential signals that are closely coupled will operate mainly in the differential mode

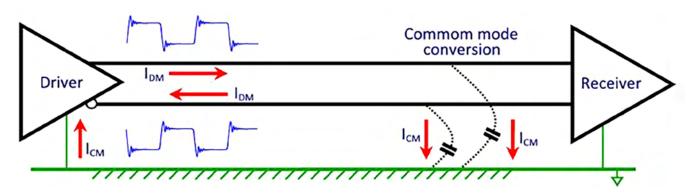


Figure 2: Differential-mode signals can be converted to common mode.

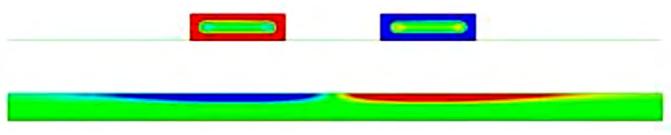


Figure 3: Coupled microstrip differential pair (courtesy Ansoft).

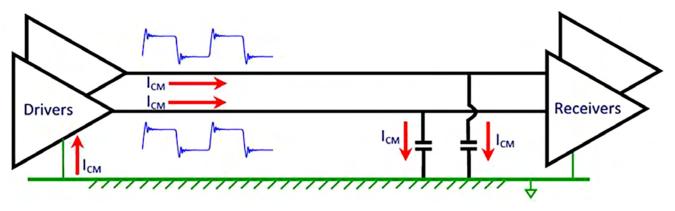


Figure 4: Common-mode signal return path.

with some common mode radiation from imbalances in the signals. If the two traces are separated enough to prevent coupling, then both act as single-ended signals. So a 100-ohm differential pair becomes two individual 50-ohm single-ended signals. This is fine, providing the loop area is small and the impedance does not change along the length of the signals.

In contrast, the "bad guy," common-mode radiation, is the result of parasitics in the circuit which emanate from the unwanted voltage drops in the conductors. As the signal is driven down the transmission line, capacitive coupling between the trace and plane conductors completes the loop and displacement current flows through the capacitance which returns to the source (Figure 4). The common-mode current that flows through the ground impedance produces a voltage drop in the digital logic ground system and generates magnetic radiation.

To make things worse, when cables are connected to the PCB, they are driven by this common mode ground potential forming antennae. In fact, it only takes 3uA of common mode current, on a 1m long cable at 100MHz, to fail an FCC Class B EMC test. Differential-mode radiation can be controlled by stackup design and routing however, common mode radiation can be difficult to understand and control because it is unintentionally designed into the system. The schematics do not show the sometimes radical, current paths taken that are vital to our understanding of signal performance, crosstalk and electromagnetic emissions.

The most prevalent form of common mode radiation emanates from cables, of the system,

that act like dipole or monopole antennae. So, it is important to limit the common mode current by:

- 1. Reducing the magnitude of the current and source voltage.
- 2. Reducing the rise-time, frequency and harmonic content of the current.
- 3. Reducing the antennae length.
- 4. Provide a common mode impedance choke in series with the cable and isolate the cable from the PCB with a transformer or optical coupler if possible.
- 5. Shield the cable and shunt the current off the cable.

The PCB power planes should not be allowed to extend into the ground area of the I/O connectors. This is because the power plane will usually contain high frequency switching noise and if extended into the I/O area, can couple the noise to the I/O signals and ground. The key here is to have a very low impedance connection, at one point only, between the I/O ground and the enclosure/chassis ground.

Also, on the PCB, microstrip stubs can act as antennae once their length approaches one quarter wavelength. These short stubs become very efficient transmitters and so are best avoided. In multi-drop buses as with DDR3/4 fly-by architecture, stubs can be avoided by routing the signals directly through each memory device pad in succession.

To control common-mode radiation, it is important to minimize the common mode ground voltage that drives the antennae at the source. PDN noise is the main driver of radiated emissions. Minimizing PDN noise is accomplished by blocking the escape of noise from the processor into the power and ground planes, and by designing a PDN that has AC impedance below the required target impedance up to the maximum bandwidth. The goal of a low impedance PDN is realized by minimizing the spacing between the power and ground planes and by using low impedance decoupling capacitors with low inductance mounting to the power/ground planes. The use of a PDN Planning tool is recommended to effectively analyze the complex requirements.

Also, good grounding minimizes noise sources by presenting common mode currents with a low impedance path to ground potential. The use of multiple ground planes, in the stackup, is a very effective way to do this. The importance of avoiding slots or splits, in the solid planes, cannot be overemphasized.

The importance of avoiding slots or splits, in the solid planes, cannot be overemphasized.

If the return path of a common mode current is far from the signal path, then the common mode current will radiate. However, if you engineer the return path to be in proximity to the source current, then the loop area will be small and therefore the common mode current will not radiate. So not all microstrip traces will radiate–just the poorly designed paths.

Key Points:

- Differential-mode radiation is equal and opposite and therefore any radiating fields will cancel.
- Common mode radiation, from two coupled conductors, is identical. It does not cancel but rather reinforces.

- Microstrip loops can act as small antennae that predominately radiate magnetic fields.
- Stripline loops only emit radiation from the fringing fields at the edge of the PCB.
- The most critical loops are the high-frequency clocks where the signal is periodic.
- Clocks should be routed on a stripline adjacent to a solid reference plane to reduce radiation.
- The spacing between the clock trace and the return plane should be as small as possible to increase coupling and reduce loop area.
- Differential mode radiation can be controlled by reducing the PDN impedance, minimizing the loop area, cancelling out the fields by using differential signals and by dithering the clocks.
- If a differential pair is not perfectly balanced, then the degree of cancellation is not determined by the spacing, but rather by the common mode balance of the differential pair.
- Differential signals, that are closely coupled, will operate mainly in the differential mode with some common mode radiation from imbalances in the signals.
- If the two differential signals are separated enough, to prevent coupling, then both act as single ended signals.
- Common mode radiation is the result of parasitics in the circuit which emanate from the undesired voltage drops in the conductors.
- When cables are connected to the PCB, they are driven by the common mode ground potential forming antennae.
- Power planes should not be allowed to extend into the ground area of the I/O connectors as noise can be coupled into the I/O signals and ground.
- Microstrip stubs can act as antennae once their length approaches one quarter wavelength.
- Stubs can be avoided by routing the signals directly through each memory device pad in succession.
- To control common mode radiation, it is important to minimize the common mode

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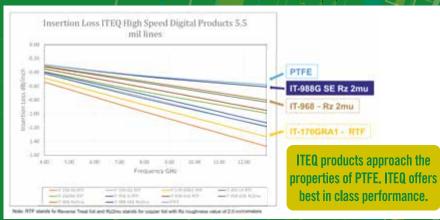
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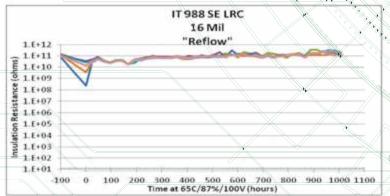


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7	Lamination cyc	le data			3115	
Lamination	DMA	DSC	TMA	1300 +10 CU	Solder Dip PCT: In St 121°C	Td Jacthi / Sarthi
1	213	187/187	182	> 80	> 60	408/435
2	216	194/199	193	/ 6a = .	> 60	41 1/438
1	214	185 / 192	185	F 60	> 60	417/442
4	216	193/194	184	> 65	> 60	434/443
5	217	1947199	190	>60	> 60	418/442
6	218	1912197 -	188	× 60	2.60	005/436
1	218	190/197	194	2.80	340	425/444

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ground voltage that drives the antennae at the source. PDN noise is the main driver of radiated emissions.

• The goal of a low impedance PDN is realized by minimizing the spacing between the power and ground planes and by using low impedance decoupling capacitors with low inductance mounting. **DESIGN007**

References

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2. Electromagnetic Compatibility Engineering, by Henry Ott.

3. What is Differential and Common-Mode Current? by Ron Brewer.

4. Understanding Common-Mode Noise, by Pulse Electronics.

5. High-Speed Signal Propagation, by Howard Johnson.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software

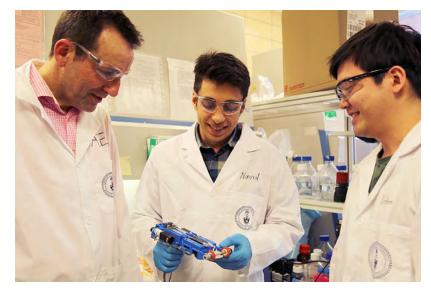
incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, click here.

Researchers Develop Handheld 3D Skin Printer

U of T Engineering researchers have developed a handheld 3D skin printer that deposits even layers of skin tissues to cover and heal deep wounds. The team believes it to be the first device that forms tissue in situ, depositing and setting in place in two minutes or less.

Their research, led by Navid Hakimi (MIE PhD candidate) under the supervision of Professor Axel Guenther (MIE, IBBME), and in collaboration with Dr. Marc Jeschke, director of the Ross-Tilley Burn Centre at Sunnybrook Hospital, was recently published in the Journal Lab on a Chip.

For patients with deep skin wounds, all three skin layers-the epidermis, dermis and hypodermis-may be heav-



ily damaged. The current preferred treatment is called split-thickness skin grafting, where healthy donor skin is grafted into the surface epidermis and part of the underlying dermis.

Split-thickness grafting on large wounds requires enough healthy donor skin to traverse all three layers, and sufficient graft skin is rarely available. This leaves a portion of the wounded area ungrafted or uncovered, leading to poor healing outcomes.

Although a large number of tissue-engineered skin substitutes exist, they are not yet widely used in clinical settings.

The handheld skin printer resembles a white-out tape dispenser – except the tape roll is replaced by a microdevice that forms tissue sheets. Vertical stripes of "bio ink," made up of protein-based biomaterials including collagen, the most abundant protein in the dermis, and fibrin, a protein involved in wound healing, run along the inside of each tissue sheet. The handheld device is the size of a small shoe box and weighs less than a kilogram.

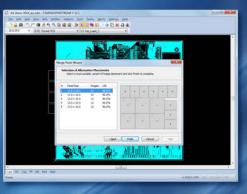
The researchers hope that one day they can begin running clinical trials on humans, and eventually revolutionize burn care.

"Several steps are needed, but we are confident we will get there," says Guenther.

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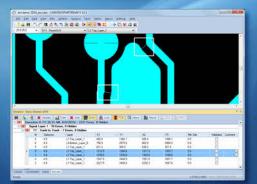


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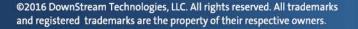


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Hiring the Right PCB Designer

Tim's Takeaways by Tim Haag, Consultant

In the movie "Seabiscuit," the story of the famous race horse, Charles Howard, Seabiscuit's owner, played by Jeff Bridges, says, "The

horse is too small, the jockey too big, the trainer too old, and I'm too dumb to know the difference."

Everyone was telling him that he couldn't make this combo work, and yet it did work, and Seabiscuit won big. If you're like me, you've probably had people tell you that something you believed in wouldn't work out, but you stuck with it and were rewarded with success.

It's easy to buck conventional thinking if you are doing something simple like painting the den in an unusual color; after all, if it doesn't work out you can always repaint it. But when it comes

to hiring new employees, it can be a lot harder to take a risk. I believe there can be great rewards when hiring managers are willing to take that risk and think outside of the standard industry box. Let me explain why.

Like the rest of you, I've had times of unemployment, when your daily job is looking for work. You find yourself writ-



ing and then rewriting your resume, searching online forums and job search sites, and applying to every job that you can find. It's particu-

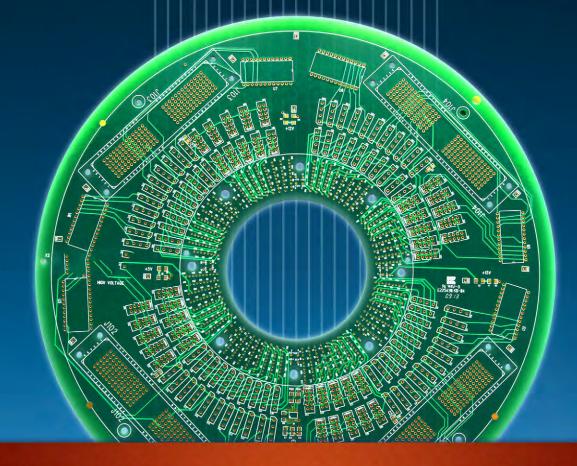
> larly tough when you find out that a job that was a perfect fit for you was filled by a less experienced person. You may have spent the last 20 years doing this job at other companies, but because you weren't fluent yet with, say, one software tool, the job was given to someone else with far less experience, but who could do this one thing.

I've hired people myself, and I know what hiring managers face. But hiring managers may be hurting their companies by drawing up a list of expectations so tight that highly qualified people may be slipping between the cracks.

I am very aware of how difficult it is for you hir-

ing managers to do your jobs. You have to follow the different rules and regulations for hiring, satisfying the legal and internal HR requirements. You also need to be able to assess multiple applicants without spending weeks or months of your time, and yet still find people who will be a good fit for the company. Being a hiring manager is a difficult job, one which





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usually doesn't get the acknowledgement and praise that it deserves. But maybe, just maybe, you could help yourself by rethinking the job requirements for the next position to open a wider range of applicants for the job.

I know skillful designers who have been turned down for a position because they don't have experience on a specific design technology, or time on a certain CAD tool. Some of these people have years and years of experience in multiple design technologies, creating some of the most intricate printed circuit boards that you can imagine, but they were turned down. There is certainly a need to find people with specific knowledge and skill sets, but the more you narrow the job requirements, the more likely you are to miss out on a real treasure of an employee.

I know skillful designers who have been turned down for a position because they don't have experience on a specific design technology, or time on a certain CAD tool.

If the job requirement is specifically for someone to design RF circuits using brand X software and this job must be producing results in the next couple of months, of course you should be searching for someone with those qualifications. If, however, you are simply increasing the staff of your design department because of anticipated growth, perhaps you shouldn't have such a tight focus on specific design experience or software skills. If your requirements are so narrow that you weed out all but those who can do one specific task, you may be missing out on someone who would have been better at doing that task once they had a little time to learn your processes. This might be

a very tough call, but I believe it should be considered.

Another thing that I have wondered about is the actual application processes. Since I just came out of a period of looking for work, I've become a guru at applying for jobs. You might think that using modern online technology to apply for jobs would be simple and easy. The reality, however, is very different. It seemed like every application I submitted had a different set of hoops that I had to jump through. Some required an attached resume, while others forced you to manually input all your personal information. Still others wanted both a resume and manual entry of personal information, and that was just the first part of the process.

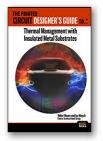
Each application also had different questions, forms, and surveys to go through, and sometimes I would have to go back to certain pages because I had missed answering a specific question or neglected checking an obscure box. It made me wonder if job candidates have inadvertently dropped through the cracks because they didn't fill out something correctly. Wouldn't it be tragic for a company that is looking for a qualified PCB designer to miss out on a stellar candidate simply because the applicant missed one of the check boxes on the online form, automatically disqualifying their application? I'm sure it happens.

The last recommendation that I would make to hiring managers would be to embrace all applicants regardless of age. It is obvious that you need to position your company for growth, and that means staffing young people who will grow with the company. On the other hand, there is a wealth of experience out there that you shouldn't ignore either. This, again, is one of those tough calls.

But consider this: According to a recent Employee Tenure Summary published by the U.S. Department of Labor's Bureau of Labor Statistics, the median number of years that wage and salary workers had been with their current employer is 4.2. This means that statistically, the young people that you hire to grow with your company will end up leaving you before they put in five years. As you drill Flexible, reliable Supply Chain Solutions high quality copper clad laminates & prepreg bonding materials



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down into the report the numbers get even more interesting; the median tenure for workers between the ages of 25 and 34 years is just under three years, while for workers ages 55 to 64 years is a little longer than 10 years.

To put it simply, if you want to hire someone young to grow with your company, it is more than likely that they will leave within a few years to continue to grow their own career and seek new challenges and opportunities. It may be tempting to avoid hiring someone who is older because you're worried that you won't get as much time with them, but again the statistics indicate otherwise.

Older workers are often happier to settle down and commit to their places of employment. You will get an employee who statistics say will stay with you three or four times as long, plus you will get the advantages of all their years of experience as well. In the end, no one knows better than you who you should be hiring for your company. You need to carefully analyze your needs and look for people that will meet those needs. My purpose here is simply to say that if you narrow your search focus too tightly, you may miss out on some great applicants.

Don't be afraid to buck industry traditions and standards when you search for new hires. As Charles Howard learned with Seabiscuit, you may find someone who doesn't meet your company's traditional criteria, but who is exactly the right person for the job. **DESIGN007**

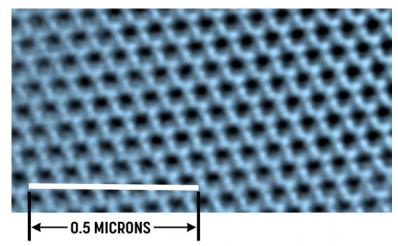


Tim Haag is a consultant based in Portland, Oregon.

Hematene Joins Parade of New 2D Materials

Rice materials scientist Pulickel Ajayan and colleagues extracted 3-atom-thick hematene from common iron ore. Hematene may be an efficient photocatalyst, especially for splitting water into hydrogen and oxygen, and could also serve as an ultrathin magnetic material for spintronic-based devices, the researchers said.

"2D magnetism is becoming a very exciting field with recent advances in synthesizing such materials, but the synthesis techniques are complex and the materials' stability is limited," Ajayan said. "Here, we have a simple, scalable method, and the hematene structure



should be environmentally stable."

Ajayan's lab worked with researchers at the University of Houston and in India, Brazil, Germany and elsewhere to exfoliate the material from naturally occurring hematite. The researchers also discovered that hematene's magnetic properties differ from those of hematite. While native hematite is antiferromagnetic, tests showed that hematene is ferromagnetic, like a common magnet. In ferromagnets, atoms' magnetic moments point in the same direction.

Unlike carbon and its 2D form, graphene, hematite is a non-van der Waals material, meaning it's held together by 3D bonding networks rather than non-chemical and comparatively weaker atomic van der Waals interactions.

> "Most 2D materials to date have been derived from bulk counterparts that are layered in nature and generally known as van der Waals solids," said co-author Professor Anantharaman Malie Madom Ramaswamy Iyer of the Cochin University of Science and Technology, India. "2D materials from bulk precursors having (non-van der Waals) 3D bonding networks are rare, and in this context hematene assumes great significance."



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Protecting PCBs from Harsh, Challenging Environments

Sensible Design by Alistair Little, ELECTROLUBE

Last month, I began my new series of columns on resins by selecting five frequently asked questions from our customers regarding resin chemistries and properties, and typical resin applications and their limitations. This month, I'm taking this introduction a step further by listing what I believe are the top five tips for circuit designers and manufacturers who seek to ensure that the reliability and longevity of their electronic assemblies and products are fully addressed.

Think very carefully about the sort of environment your PCB is likely to encounter. It is easy to over-engineer a product so that it will survive the very worst of conditions, but worst conditions may only be fleeting or transient. Therefore, a resin solution with a lower temperature performance specification will often cope. Take temperature extremes, for example. Your application may experience occasional temperature spikes of up to 180°C, which you might feel deserves treatment with a special resin. However, such excursions may only be short-lived; under normal operating conditions, the PCB might only be subjected to a maximum temperature of, say, 120°C, opening a wider choice of resin types and methods of application.

In a similar way, the required chemical resistance of your chosen resin will depend on the duration and/or extent of the chemical contamination. For example, there is a considerable difference in terms of the extent of chemical damage between a thin layer of a contaminating chemical on the resin surface that is wiped off within five minutes and 500ml of chemical present on the resin surface for one hour or more—let alone complete immersion! Furthermore, the range of chemicals that a PCB might



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eventually be exposed to is often quite limited, and almost certainly not the broad range that is frequently listed at the design stage, just to be on the safe side.

2 Environmental factors that normally affect a PCB are temperature, chemical attack, physical shock (vibration) and thermal shock; the trick is to decide which of these is likely to have the greatest impact upon your PCB and then concentrate on making an appropriate resin choice. Each of the three main resin types (epoxy, polyurethane and silicone) have strengths and weaknesses.

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Silicone resins have the broadest continuous operating temperature range of any of the resin chemistries, so they are a natural choice for both high- and low-temperature applications, as well as those subject to thermal shock. They also maintain their flexibility over this temperature range with very little sign of degradation over time. On the downside, silicones have poor adhesion on certain substrates and their chemical resistance is not as good as that provided by an epoxy resin.

As well as having excellent chemical resistance, epoxies provide good temperature performance. However, due to their rigid nature, epoxies are not so good at protecting against physical shock. Polyurethanes, on the other hand, have excellent moisture and physical shock resistance, but deliver poor high-temperature performance. As a result, polyurethanes are best restricted to applications operating in the -40 to + 120°C region. They do, however, provide similar levels of flexibility and better adhesion to many substrates compared with silicones, and at a lower cost.

Where the PCB is mounted in an enclosure into which resin is poured to fully encapsulate it, the material that the enclosure is made from needs to be taken into consideration. In the case of plastic enclosures, these are normally injection moulded, so there might be traces of release agent on the surfaces that will result in poor resin adhesion unless the agent is removed beforehand. Some plastics are very moisture sensitive and are likely to undergo dimensional and other physical changes in humid conditions, which will impose physical stresses on the enclosure, the encapsulation resin, the PCB and the components. Where the enclosure is made from steel, aluminium or other metals, then the differences in the coefficient of thermal expansion between the enclosure and the resin will have to be considered, as well as the surface treatment used, which might affect the adhesion of the resin.

Typically, the thicker the resin layer, the better the level of protection; however, unless all the components on the PCB are of a uniform height, then the thickness of the resin layer will vary across the board, and potentially slightly different levels of protection will be provided for individual components. Good board design and component selection will go a long way towards mitigating this type of problem, but the thinnest resin layer must be assumed to be the level of protection offered across the board. Naturally, with the desire/ need to reduce weight and/or volume, designers are inclined to reduce the amount of resin applied. Nonetheless, the expected service life needs to be factored in, with thicker layers generally providing better long-term protection.

5 Just remember, before you even consider resin encapsulation or potting, the PCB needs to be thoroughly cleaned. Surface contamination can have a negative impact on the protection levels offered by encapsulation, particularly in cases of chemical resistance (as it provides an easier route for chemicals to penetrate). In addition, contaminants will adversely affect the resin's ability to absorb physical and thermal shocks due to the weak layer forma-

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tion between the resin and the PCB, which ultimately leads to delamination. Of course, after cleaning, any solvent or cleaning solution must be removed, and the PCB needs to be thoroughly dried prior to resin application.

By paying attention to these basic design pointers, you are likely to achieve the levels of reliability and long service life that will ensure long and happy relationships with your customers! Over the coming months, I shall be looking at a wide range of issues concerning the correct choice and application of resins, so be sure to check out this column in future issues. **DESIGN007**

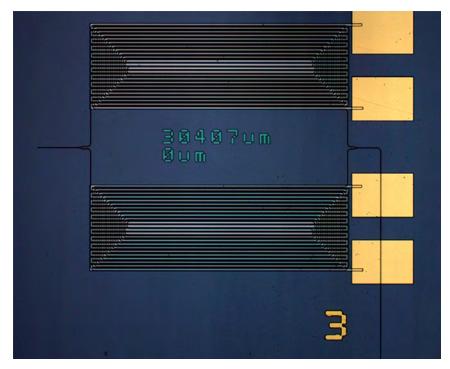


Alistair Little is the global business/technical director for the Resins Division of Electrolube.

Infrared Spectrometer on a Chip

Fourier-transform infrared (FTIR) spectrometers are too large to be used in the field to detect compounds. Several attempts have been made to develop miniaturized FTIR spectrometers for integration into drones to monitor greenhouse gases remotely, for example, or for integration into smartphones and other devices. However, current miniaturized devices are costly to produce and therefore cannot be widely used.

Scientists at the University of Campinas's Device Research Laboratory (LPD-UNICAMP) in Brazil, collaborating with colleagues at the University of California San Diego, have overcome these constraints by developing an FTIR spectrometer based on silicon photonics, the technology currently used to produce chips for comput-



ers, smartphones and other electronic devices.

Resulting from Mário César Mendes Machado de Souza's PhD research and a research internship abroad, supported by scholarships from FAPESP and supervised by Professor Newton Frateschi, the new spectrometer is described in an article published in Nature Communications.

According to Souza, FTIR spectroscopy identifies chemicals using an infrared light source to measure absorption. A sample is exposed to different wavelengths of infrared light, and the spectrometer measures which wavelengths are absorbed. The computer takes these raw absorption data and conducts a mathematical process known as the Fourier transform to generate an absorbance pat-

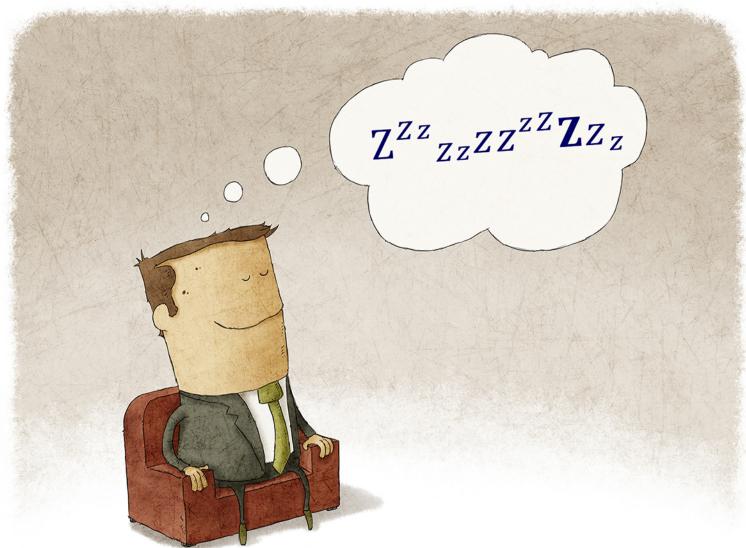
> tern or spectrum, which is compared to a library of spectra for chemical compounds to find a match.

> Various projects have appeared in recent years to develop an FTIR spectrometer based on integrated photonics, which uses light especially in the infrared spectrum, but progress had so far been scant owing to several technical challenges, Souza explained.

> One of these challenges is the highly dispersive profile of silicon waveguides, meaning that each wavelength travels at a different speed in this material and hence has a different refractive index.

> The researchers now plan to engineer a device that is totally functional and integrated with photodetectors, light sources and optical fibers.

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Arlon EMD Achieves IPC's Qualified Product Listing Certification >

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TTM Technologies Completes Acquisition of Anaren >

TTM Technologies Inc. announced that it has completed its acquisition of Anaren, Inc. The combined company had pro-forma 2017 revenue of \$2.9 billion.

Microtek Laboratories China Completes First U.S. IPC-4101E Validation Services Test Program ►

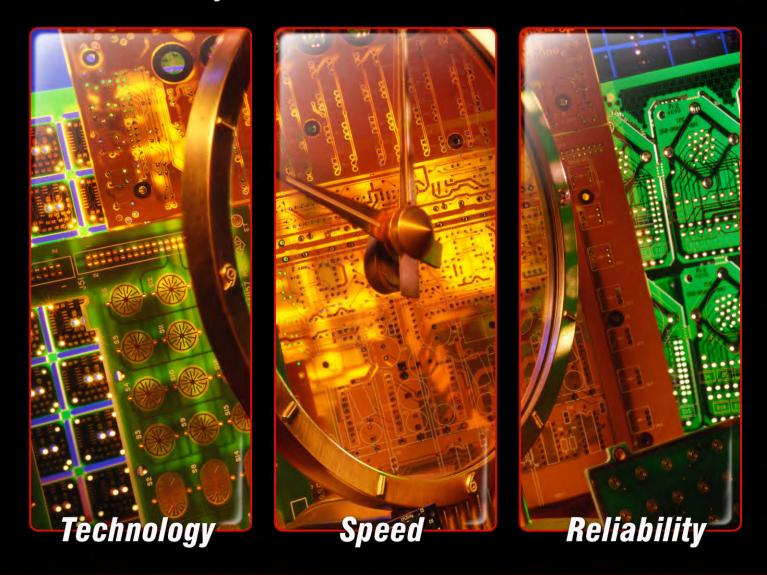
Microtek Laboratories China has completed the first qualification testing program for IPC-4101 Validation Services for a U.S. manufacturer of copper-clad laminates and prepreg.

Lockheed Martin and Cobham Team to Develop Next Gen Jammer Low Band for U.S. Navy's Electronic Warfare Aircraft ►

Lockheed Martin and Cobham are joining forces for the Next Generation Jammer Low Band (NGJ-LB) competition to replace the U.S. Navy's ALQ-99 tactical jamming system currently on the E/A-18 Growler aircraft.

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Mark Thompson: What Designers Need to Know about Fab

by Dan Beaulieu

Mark Thompson wants to help PCB designers. He's seen it all in CAM support at Prototron Circuits: the incomplete or inaccurate data packages, boards that are unnecessarily complex or over-constrained, and so much more. As technical customer liaison, Mark leads tours of Prototron's facility in Redmond, Washington, often providing PCB designers and design engineers their first glimpse inside a board shop. Mark just returned to writing his popular *Design007 Magazine* column, *The Bare (Board) Truth*, which addresses questions such as, "What happens to your design at CAM?"

I've known Mark for years, and it's always a pleasure to get a chance to talk with him. In our interview, I asked Mark to explain why it's so important for designers to communicate with their fabricators, and why they need to get out of the office and visit a board shop every now and then. **Dan Beaulieu:** Good morning, Mark. Good to see you again. I have a few questions for you.

Mark Thompson: Fire away!

Beaulieu: So, why should PCB designers talk to board shops?

Thompson: Excellent question, straight to the point. The answer is, because designers need to understand fabrication needs, and we as fabricators need to know their needs. Since we primarily deal with prototypes here at Prototron, most of the parts we see are first-run prototypes, and we have the potential to find unforeseen errors that need to be aired out before production.

Board applications have changed so vastly over the years that it is difficult, if not impossible, for a fabricator to attempt to guess at a customer's intentions. Nor should he try! That's where a simple conversation between

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the board designer and the board fabricator can be invaluable. For example, a customer may ask me questions like these: "Mark, what is the smallest mechanical hole size you can do?" Or "What is the thinnest dielectric you can deal with?" Or, "What is the minimum solder mask clearance you need?"

All are perfect examples of questions that, depending on the customers' intentions, and they can be answered in multiple ways. The first question, asking about minimum mechan-

ical hole size, is usually followed by "What is the smallest signal pad associated with that hole size and what is the smallest anti-pad on a plane layer for that hole size?" This is where the fabricator should be asking more questions, such as, "Are you referring to vias when you ask about our smallest hole size?"

Because you can buy yourself back a lot of real estate for trace routing, smaller pad sizes

and smaller anti-pad sizes by your tolerance callout. If you call them out as +/-.003" we must drill some .004-.005" mils larger than the nominal hole size to plate back down to the nominal. If all you want is electrical continuity and don't really care how small a given via ends up, call it out as +.003" minus the entire hole size. This tells a fab shop that they can drill the hole smaller, which makes my answers about minimum pad and minimum anti-pad size more appealing. They can now be smaller.

The same holds true with the second question. I need more information on my part to adequately answer this question. Sure, I can tell you we can use .0025" core internally for capacitance and decoupling, but can we have .0025" pre-preg dielectric between 1 oz. clad cores? No! And that is where my conversation changes to copper aspect ratios and pre-preg nesting or loss due to the layer type. Is it full plane, where it may not lose a lot of dielectric distance, or a signal where it may lose some dielectric?



Mark Thompson

Let's talk about the third question regarding minimum solder mask web. If you ask me what solder mask clearance we prefer for a given pad or SMT, we will tell you about .003" per side or .006" total over the signal pad size. But you have to understand that this is not always feasible, depending on board geometry! That is where we can talk about less clearance to be able to maintain the minimum web size between mounts. Beyond any tolerance or capability questions, your board fabricator

> has empirical data to support the Dk numbers that they use to meet a customer's given impedances. Many times, we are at least a decimal point past what the material manufacturer says, all in an effort to get the customer what they want.

> There are a lot more reasons a designer may want to talk with a fabricator, but it really boils down to that first statement. Our customers, the designers,

need to understand fabrication needs. And we as fabricators need to know their needs.

Beaulieu: Sounds like there are a lot of reasons for a board designer to speak with a board fabricator.

Thompson: Absolutely.

Beaulieu: Changing gears a little, what are some things that can make the price of boards go up un-necessarily?

Thompson: That's a good one! There are a number of things that can make the price of a part go up. I guess it really comes down to how close the customer wants to get to the finalized product with a prototype. Is the build for part fit/assembly, or functionality, or both? If it's only for part placement and fit, they may decide to build the part on a material much less costly than the one they will end up with in the final product. They may even choose not to have an image, mask, or ID depending on

the purpose of the build, or conversely, they may want to check all functionality via a network analyzer. In that case, you cannot sub materials.

Beaulieu: Those are great for folks who are just prototyping, but are there other ways to save cost?

Thompson: Yes, sometimes it comes down to technology. I see a lot of jobs set up as blind

vias, for instance, that do not need to be blind vias. This happens on boards with tons of additional routing space and adequate distance between points internally for standard through-hole interconnects. Why use blind vias unless you absolutely have to?

Beaulieu: Last question. What are some things that designers may not know about board shops that they really should know?

Thompson: Ha! There are probably thousands of such things. I would say that designers not understanding manufacturing edits or not providing an IPC netlist are the things that can bite a customer the most. Some things that are frequently not considered as far as necessary manufacturing edits are etch compensations and drill compensations.

For every half ounce of starting copper, meaning prior to plating, we add a half a mil etch compensation to account for the known loss at our etcher. So, starting on half ounce with .005" trace and space, the image data, whether it is artwork or direct image electronic data, would be at .0055" traces with .0045" spaces prior to etch after image. These compensations cannot take the fab house below their process minimums. So, the same .005" traces with .005" spaces would not be possible if the customer asked for three oz. copper, as the image data would be below the shop's minimum space after etch compensation. Additionally,



Dan Beaulieu

Class 3 6012 /AS9102 parts that have epoxy fill or blind vias will require additional wrap plating to encapsulate the pad. This too needs additional space metal-to-metal and should be accounted for in the design.

Similarly, for drills we do a compensation so that after through-hole plating the drills end up as the nominal size specified on the drawing. This means that if you call out a component hole as .008" + /-.003" and only have .010" signal pads after drill compensation, we would

drill those same .008" holes at approximately .0138" so a .010" pad would be insufficient. In fact, to even get close to meeting IPC the pad size should be closer to .020".

If you have designed for .010" pads and a manufacturer tells you that you need to double that number for an .008" drill, for you as the designer, that means a whole new layout. Again, if the holes are being used for plug-in components,

the fab shop cannot reduce the hole size to deal with the pad size. However, if meeting IPC/AS9102 is not necessary, sometimes the board shop will say that they can live with a smaller pad size as a compromise, so that it may not require an entirely new layout.

Beaulieu: Any last thoughts, Mark?

Thompson: Lastly, remember that the best way to make sure the part functions electrically as designed is to provide an IPC netlist of your design criteria to be run against your provided image data to make sure they are electrically the same. Word to the wise about netlists: Avoid assigning net points to things like targets, moirés, non-plated holes or castellated holes.

Beaulieu: Thanks, Mark. Great seeing you again.

Thompson: Thank you, Dan. It's been a pleasure. **DESIGN007**

Faster Board Speeds Demand Constraint-Driven Design

by Ralf Bruening ZUKEN

> Do you still use Post-it Notes? Invented in 1979, this simple, yet incredibly powerful communication mechanism is

> > still commonly found in engineering and design departments. Despite modern electronic communication, many companies

still struggle to provide a replacement for their ease-of-use and versatility.

But, by changing the way an engineer designs electronics, by giving up the Post-it for passing requirements, change requests and constraints between engineers, design times can be shortened and product quality improved. Modern PCB design tools permit the definition of design constraints, including constraints relating to high-speed design and EMC, such as the topology of connections (routing pin sequence) or overshoot and timing budgets, for example.

These constraints become increasingly important as components and boards become faster and more complex. But it is hard to capture and use/obey these constraints consistently throughout the complete design process, bearing in mind that may contradict each other. The Post-it Note captures this idea particularly well. A brief sketch implicitly includes the



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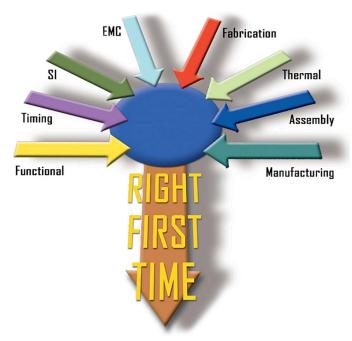


Figure 1: Typical PCB-related design constraints.

constraints that the designer is working under, in a very concise form; however retaining and using this information later is extremely difficult.

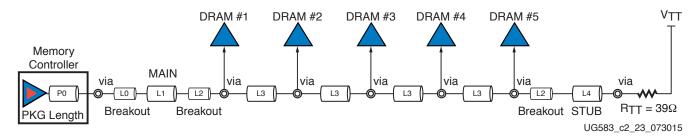
Adaptive Design

Using these powerful constraint techniques can be a double-edged sword. While the design process is made much safer by including constraints, it is all too easy to over-constrain the design and make it impossible to complete routing and placement. Even paper design guidelines can make products uneconomic to produce unless a great deal of engineering knowledge is applied during the design. This means the design tool has to be adaptive—reacting to changes in the design as it progresses. Combining these elements is anything but trivial, but doing so allows the designer to converge on the optimum design in the first pass, rather than via multiple attempts.

In PCB design, attributes (or constraints) and rules have always existed, and designers have tried to achieve their design goals, especially with systems that are based around the raw attributes of the components in a design. But attributes (or properties) are essentially just data about the pins, components or tracking, while constraints are requirements that must be obeyed. Examples include the maximum delay, or an error marker, which must be flagged as functional or an operation may be at risk. These can simply be a function of the design attributes, but constraints are typically more complex nowadays and they sometimes relate to each other (e.g., in high-speed memory the relationship between the byte lanes and from the data/address signals to strobe and clock signals). Constraints must exist through

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E- ADD(10)	10	-ADO(10)								60.00000	
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Figure 2: Example of a constraint browser, the Zuken CR-8000.



Parameter	L0 (Device Breakout)	L1 (Main PCB)	L2 (DRAM Breakout)	L3	L4 (To R _{TT})	Units
Trace type	Stripline	Stripline	Stripline	Stripline	Stripline	-
Single-ended impedance Z ₀	50±10%	36±10%	50±10% 50±10% 39±10		39±10%	Ω
Trace width	4.0	7.0	4.0	4.0	6.0	mil
Trace length	0.0~1.5 ⁽¹⁾	0.0~4.0	0.0~0.1	0.35~0.75	0~1	inches
Spacing in address, command, and control signals (minimum)	4.0	8.0 ⁽¹⁾	4.0	8.0	8.0	mil
Spacing to clock signals (minimum)	8.0	20	8.0	20	20	mil
Spacing to other group signals (minimum)	8.0	30	30	30	30	mil
Maximum PCB via count			7	•		-

Notes: 1. If greater than 1.5 inches is needed in the breakout area, change L1 spacing to 12.0.

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3	E DOR4-FlyBy	Node2-Node9	TL14		25,40000			6mil		35.00000	44.00000
4	E DOR4-FlyBy	Node5-Node6	TL6	8.85000	19.05000			4mil		45.00000	55.00000
5	E DOR4-FlyBy	Node5-V8P2	TL4	25.40000	112.00000			7mil		32.00000	40.00000
6	E DOR4-FlyBy	Node6-Node7	TL8	8.85000	19.05000			4mil		45.00000	55.00000
7	E DOR4-FlyBy	Node7-Node8	TL10	8.85000	19.05000			4mil		45.00000	55.00000
8	E DOR4-FlyBy	Node8-Node9	TL12	8.85000	19.05000			4mil		45.00000	55.00000

Figure 3: JEDEC DDR4 topology rule and equivalent CR-8000 topology template.

the different stages of the design process, from schematic to placement to routing.

Space to Experiment

One of big issues that engineers have typically run up against is that the experimentation environment (the Post-it Note, to continue our analogy) was kept separate from the design process. While the two tasks are often performed separately, it is also vital to be able to transfer the constraints developed in these virtual designs into the real-world design once they are judged appropriate.

Modern EDA tools take this approach, with a constraint managing mechanism holding the constraint data of a design from schematic to manufacturing. The designer can then navigate through the constraints and modify them. The key issue with this approach is to get the constraints into the database without having to type in lots of numbers and data. Another important aspect to consider is that constraints not only have an impact on the physical realization of a design, but also impact the electrical signal quality and noise behavior.

Graphical topology editing, with constraintsetting including the capability to assign topologies to nets or groups of nets, allows easy constraining with inheritance. Real routing topology extraction and scratchpad editing allow the designer to look at "what if" designs, much like the drawings on the back of the Post-it Note.

For instance, what if a memory bus runs at twice its current speed, or a transmission line length is halved? The vital part of the system is that design snapshots (scenarios) can be verified against the constraints and detached from the rest of the real system design as it develops, then be automatically transferred into the constraint database. Those "what-if" scenarios may behave like a small design on their own; they can be analyzed in the same way for parameters, including signal speeds, crosstalk and distortion. The constraints worked out from such simple sub-design elements can be fed back into the constraint database, thus closing the design loop.

It is very important that constraints can be passed/attached at electrical nets (including series passive components like capacitors and resistors), and groups of nets (e.g., buses and net classes) rather than just on a single particular net. This is a great advantage in the constraining process, as defining constraints for larger systems can then be carried out much faster. Constraints can be reused by importing/ exporting in standard formats such as .XML or .CSV (Figure 4).

Closing the Design/Simulation Loop

Beside geometrical constraints like net length and spacing, these days electrical requirements such as dedicated delay, delay difference (= skew) or distortion/overshoot have to be met. Signal integrity simulation is much more accurate than using formulas for delay and overshoot evaluation. A key part of the process of constraint-driven design is to have simulation available throughout the process to determine whether the constraints are met. This requires a fundamental change in the architecture of the tool.

Traditionally, SI simulation has been a postlayout process, done after a design has been laid out or the routing determined. With modern constraint-driven tools, the simulation engine is tightly integrated in each operation/ phase of the design flow. SI verification can be performed in both the time-domain and the frequency-domain. Time domain simulation has advantages when modeling non-

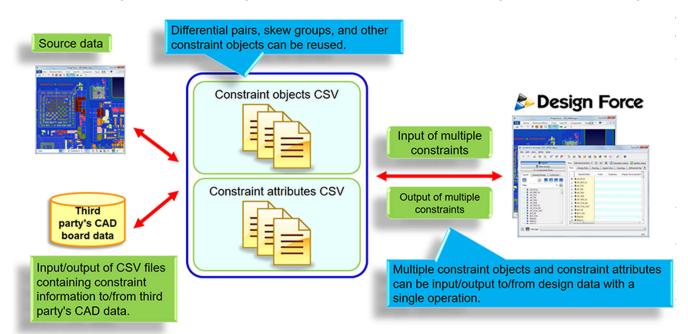


Figure 4: Import/export of constraints.

Medical Electronics Symposium 2018 May 16 & 17

University of Texas at Dallas • Dallas, TX

SMTA, INEMI, and MEPTEC have joined forces to again host this international conference, focusing on advances in electronic technologies and advanced manufacturing, specifically targeting medical and bioscience applications. Our last conference attracted about 200 attendees and more than 30 exhibitors. In prior years, MEPTEC's and SMTA's conferences were held in Phoenix, AZ and Milpitas, CA, respectively, drawing technology experts, entrepreneurs and service providers that work in this niche technology space. Typical applications within this space involve implantable defibrillators, neurostimulators and drug delivery, interventional catheters, pillcams, ultrasound transducers, hearing aids, biosensors, microfluidics, wireless communications, as well as future diagnostic and treatment solutions that may use stretchable electronics, microelectromechanical systems (MEMS). ◆

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Unlocking the Value John Burnes, Medtronic Technical Fellow Director of Implantable Core Teams Cardiac Patient Monitoring and Diagnostics Medtronic

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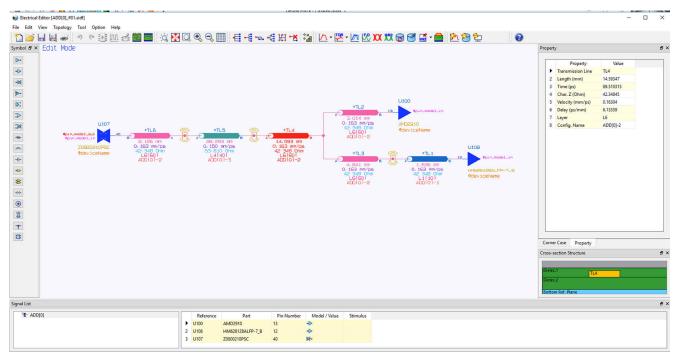
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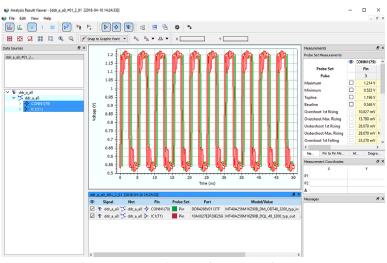


Figure 5: Signal integrity simulation of a net topology.

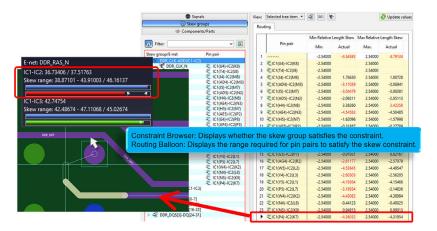


Figure 6: Communication between constraint management and layout.

linear active components; frequency-domain simulation tends to be better at modeling the effects of capacitance and inductance.

As board speeds increase, the significance of capacitance and inductance tends to increase relative to that of non-linear device characteristics, but with tools such Zuken's CR-8000, engineers as can choose which domain to simulate in, depending on the analysis focus. During the routing, this means that each element of track can be simulated as soon as it is routed, with the results fed back to the router. This means that the routing solution converges on a value that is within the constraints, rather than having to redo some, if not all, of the routing if one part is found to fall outside the constraints when the design is re-simulated after routing. Real time communication between the constraint browser and the routing engine (Figure 6) allows the engineer to optimize routing results in an efficient manner.

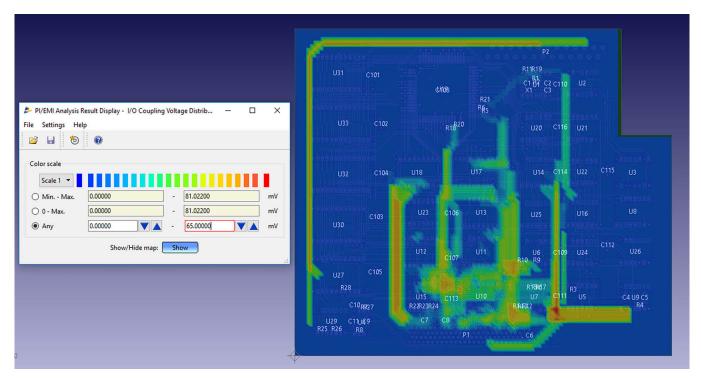


Figure 7: Embedded fast EMI verification of PCBs.

Constraining for EMC/EMI

Next, constraints concerning the electromagnetic compatibility capability (EMC/EMI) of a design need to be considered in a similarly integrated way as the signal integrity, thermal and manufacturing issues. However, this poses a slightly different set of problems. Because EMI is closely related to the physical layout of the design, any analysis is only valid once the design has reached the physical stage. So for efficient design verification, algorithms developed with the University of Missouri-Rolla (now Missouri University of Science and Technology) have been implemented into a fast EMI worst-case prediction checker (Figure 7).

This allows an EMI analysis on differential and common mode noise (such as parasitic antennae and I/O coupling) at given frequencies, as well as analysis of radiation from power planes, including decoupling analysis. Such an approach is better suited to a concurrent PCB design process, rather than traditional full wave numerical EM analysis approaches.

But there is always the risk of over-constraining, rendering a design unbuildable or economically unviable. The engineering trade-offs in the number of layers, manufacturing technology required for fabrication of the board, and the parameters for assembly are complex and have to be agreed by the designer in conjunction with the production team. When consensus is reached, the EDA system needs to be flexible enough to accommodate these parameters in the technology files that form part of the design database.

All of this might seem a like lot to replace a simple piece of paper, but this addresses problems that have held back constraint-driven design over the last couple of years. Tools such as the CR-8000 now provide engineers with a practical constraint-driven design approach. What used to require a multi-tool and often a multi-vendor, mix-and-match system, is now possible with a single, coherent modern design tool allowing constrained-driven design on single-board and multi-board systems in both 2D and 3D. **DESIGN007**



Ralf Bruening is a product manager and senior consultant at Zuken's EMC Technology Centre in Paderborn Germany, focused on Zuken's high-speed design, SI & EMI verification tools.



Recent Highlights from Design007

■ Fadi Deek Discusses Mentor's New Power Integrity eBook ►

At DesignCon 2018, I ran into Mentor's Fadi Deek, the author of both of Mentor's I-007eBooks. We sat down and discussed how the idea for the books came about, as well as some of the



IOP

power integrity challenges facing PCB designers and engineers.

2 Ucamco Releases Specification for Fabrication Documentation in Gerber ►

The Gerber Job File is straightforward to implement. Partial implementations are allowed, even encouraged. Better a partial job file than no job file at all. Developers can pick and choose from the spec what suits them. Several software suppliers have already committed to support the new Gerber Job File.

3 Zuken Pulling Ahead in Automotive PCB Design ►

Zuken has been developing PCB design tools for the automotive market for years. With automotive electronics worth over \$200 billion globally, and growing every day, Zuken is preparing for a brave new world of smart cars, and autonomous and electric vehicles. I spoke with Humair Mandavia, chief strategy officer with Zuken, and asked him about the challenges facing automotive PCB designers, and the trends he's seeing in this constantly evolving segment of the industry.

4 Cadence Reports Q1 2018 Financial Results ►

Cadence Design Systems, Inc. reported its results under new revenue rules, ASC Topic 606, for the first time. For the first quarter of 2018, Cadence reported revenue of \$517 million, GAAP net income of \$73 million, or \$0.26 per share on a diluted basis, and non-GAAP net income (as defined below), of \$113 million, or \$0.40 per share on a diluted basis.

5 The Bare (Board) Truth: Refining Output Data Packages for Fabricators ►

One of the biggest issues PCB fabricators face is the completeness (or incompleteness) of the data output package we receive from customers on a new PCB. In this column, I am going to present what is



needed, from a fabricator's perspective, for a good output package and why.

6

Polar Instruments Launches Speedstack Si 2018 Edition ►

Polar Instruments, a specialist provider of tools for PCB design, fabrication and test, announces a major enhancement for Speedstack Si. Speedstack Si 2018 edition now incorporates the industry standard Polar Si9000e integrated insertion loss field solver engine – which lets the user both design and add comprehensive insertion loss graphs and stackup specification into Speedstack's professional report printer.

Will Cool Technology Attract the Next Generation of PCB Designers? >

We live in an increasingly connected world. Ben Jordan of Altium recently theorized in these pages that there could be more than 200,000 new designs required to fulfill the needs of the 20 billion connected



devices projected to be in use by the year 2020. Yes, you read that correctly, 20 billion connected devices.

8 RUSH PCB Unveils 10-Layer HDI Design and Manufacture Capabilities ►

Rush PCB Inc. now offers the design and manufacturing of multilayer HDI PCBs of 10 layers and more. In making the announcement, CEO Akber Roy stated, "To achieve very high-density interconnection, designers at Rush PCB Inc. use what we know as Every Layer Interconnect (ELIC) technology. This is a method wherein each layer has its own copper-filled laser-drilled microvias. When stacked up, it provides the opportunity for dynamic connections between any two layers in the PCB.



A capacitor is typically placed in series with both differential signal traces to remove common mode voltage differences between ICs or different technologies. An "AC coupling capacitor" or "DC blocking capacitor" basically refers to the same thing. Any capacitor placed in series with the signal path tends to pass the high-frequency, AC portions of the signal, while simultaneously blocking the low-frequency DC portions. Since these capacitors couple transmitter to receiver, I prefer to use the term "AC coupling."

■ Porsche Engineering...by Design ►

Thomas Wischnack of Porsche Engineering is currently designing the high-power charging infrastructure that will go inside the next generation of automobiles. Thomas was a keynote speaker at AltiumLive 2017 in Munich, Germany. I met with him to learn more about Porsche's hardware and circuit development and what Porsche does to continually bring new designers into the fold.

PCBDesign007.com for the latest circuit design news and information—anywhere, anytime.

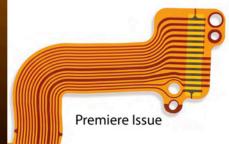


FLEXOOT MAGAZINE

Quarterly | April 2018

Got Flex?

Flex007 Magazine is dedicated to flex system designers, electrical engineers, flex PCB designers, and those responsible for integrating flex into their products at the OEM/CEM level.





Flex007 Magazine is dedicated to flex system designers, electrical engineers, flex PCB designers, and those responsible for integrating flex into their products at the OEM/CEM level.

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TAIYO KOGYO CO., LTD.

New Business Development Representative for USA market

Taiyo Kogyo is a Japanese PCB manufacturer. We started manufacturing PCBs in 1962, and have unique and differentiated boards used in various industry segments. Our products are appreciated for application in power electronics. High current PCB and thermal solution PCBs are our strength.

Position Summary:

Responsible for creating new business and expanding business with existing customers in the U.S. Work at your home office. Part-time (half-day/ 5 days a week) okay. (Option: After first 6 months, job can be upgraded for full-time work based on performance.)

Responsibilities:

- Develop new customers: Work closely with local sales representatives and independently in territories without sales reps.
- Educate and support local sales representatives.
- Operate as company's U.S. Sales office and communicate daily with Japanese headquarters for smooth and speedy communications with local sales reps and customers.
- Travel and visit prospective customers with local sales reps or alone to develop new customers (about 6 to 10 times a year).
- Attend company booth at business expo (APEC) during the show.
- Search for and appoint competent local sales reps in non-covered regions.



Technical Support Engineer, UK

As a UK-based Technical Support Engineer, you will help customers choose and optimize the use of Ventec materials in their Printed Circuit Board manufacturing processes. You will provide a two-way channel of technical communication between Ventec's production facilities and UK/European customers. You will be required to undertake some laboratory testing (including the use of TMA, DSC, Melt Viscometer, Gel Plate Timer, and laboratory scale multilayer presses) and provide appropriate technical support to Ventec UK and European sales personnel to maximize results.

Skills and abilities required for the role:

- Hold a HNC, HND, degree or equivalent in a technical/scientific discipline.
- Excellent communications skills and ability to write full technical reports for group or customer distribution.
- Ability to work in an organized, proactive, and enthusiastic way.
- Ability to work well, both in a team as well as an individual.
- Good user knowledge of common Microsoft Office programs.
- Full driving license essential.

Appropriate training will be given if required.

This is a fantastic opportunity to become part of a successful brand and leading team with excellent benefits. For more information, please click here.

> Please forward your resume to HR@ventec-europe.com.

> > apply now



PCB Manufacturing, Marketing Engineer

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, tradeshow, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

Â.

American Standard Circuits

Creative Innovations In Flex, Digital & Microwave Circuits

Front-End CAM Operators

Chicago-based PCB fabricator American Standard Circuits is currently seeking frontend CAM operators to join their team. Desired applicant will have three years of CAM experience.

The candidate should also possess:

- Expertise in Valor/Genesis CAD/CAM software and PCB process
- Ability to process DRC/DFMs
- Excellent customer/people skills
- Ability to be a self-starter
- Ability to read prints and specifications

American Standard Circuits is one of the most diverse independent printed circuit board fabricators in the country today, building PCBs of all technologies, including epoxy MLBs, flex and rigid-flex, RF and metal backed.

To learn more about this position, please send your information to American Standard Circuits.



Technical Service Rep, Northeast

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Technical Service Rep will be responsible for day-to-day support for fabricators using MacDermid Enthone's chemical products. The position requires a proactive self-starter who can work closely and independently with customers, sales group members and management to ensure that customer expectations and company interests are served.

- Thoroughly understand the overall PCB business, and specifics in wet processing areas
- Prepare action plans for identification of root cause of customer process issues
- Provide feedback to management regarding performance
- Create and conduct customer technical presentations
- Develop technical strategy for customers
- Possess the ability to calm difficult situations with customers, initiate a step by step plan, and involve other technical help quickly to find resolution

Hiring Profile

- Bachelor's Degree or 5-7 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Extensive experience in all aspects of customer relationship management
- Willingness to travel

apply now



KYZEN Regional Manager – Midwest Region

General Summary: KYZEN is seeking a Regional Manager to join our sales team in the Midwest. This position is ideally suited for an individual that is self-motivated, hard-working and has a "whatever it takes," positive attitude, especially with customers. Being mechanically inclined is a plus. KYZEN will provide on-going, in-the-field training to help you succeed.

CORE FUNCTIONS:

- Collaborates with the Americas Manager in establishing and recommending the realistic sales goals for territory
- Manages the assigned geographic sales area to maximize sales revenues and meet corporate objectives
- Develops sales strategies to improve market share in all product lines (Electronics and Industrial)
- Ensures consistent, profitable growth in sales revenues through planning, deployment and management of distributors and sales reps as well as continued direct support for customers and prospects processes

REPORTING:

• Reports directly to Americas Manager

QUALIFICATIONS:

- A minimum of seven years related experience or training in the manufacturing sector or the equivalent combination of formal education and experience
- Excellent oral and written communication skills
- Working knowledge of Microsoft Office Suite
- Mechanically inclined a plus
- Valid driver's license
- Travel within the region up to 75% of the time with occasional travel outside the region



Ventec INTERNATIONAL GROUP 勝輝電子

Ventec Seeking U.S. Product Manager for tec-speed

Want to work for a globally successful and growing company and help drive that success? As a U.S.-based member of the product and sales team, your focus will be on Ventec's signal integrity materials, tec-speed, one of the most comprehensive range of products in highspeed/low-loss PCB material technology for high reliability and high-speed computing and storage applications. Combining your strong technical PCB manufacturing and design knowledge with commercial acumen, you will offer North American customers (OEMs, buyers, designers, reliability engineers and the people that liaise directly with the PCB manufacturers) advice and solutions for optimum performance, quality and cost.

Skills and abilities required:

- Technical background in PCB manufacturing/ design
- Solid understanding of signal integrity solutions
- Direct sales knowledge and skills
- Excellent oral and written communication skills in English
- Experience in making compelling presentations to small and large audiences
- Proven relationship building skills with partners and virtual teams

This is a fantastic opportunity to become part of a leading brand and team, with excellent benefits.

Please forward your resume to <u>jpattie@ventec-usa.com</u> and mention "U.S. Sales Manager—tec-speed" in the subject line.



Field Service Technician

Chemcut, a leading manufacturer of wetprocessing equipment for the manufacture of printed circuit boards for more than 60 years, is seeking a high-quality field service technician. This position will require extensive travel, including overseas.

Job responsibilities include:

- Installing and testing Chemcut equipment at the customer's location
- Training customers for proper operation and maintenance
- Providing technical support for problems by diagnosing and repairing mechanical and electrical malfunctions
- Filling out and submitting service call paperwork completely, accurately and in a timely fashion
- Preparing quotes to modify, rebuild, and/or repair Chemcut equipment

Requirements:

- Associates degree or trade school degree, or four years equivalent HVAC/industrial equipment technical experience
- Strong mechanical aptitude and electrical knowledge, along with the ability to troubleshoot PLC control
- Experience with single and three-phase power, low-voltage control circuits and knowledge of AC and DC drives are desirable extra skills

To apply for this position, please apply to Mike Burke, or call 814-272-2800.

apply now



IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.



Account Manager, Northeast

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of Account Manager will be responsible for selling MacDermid Enthone's chemical products. The position requires a proactive self-starter who can work closely and independently with customers and sales management to ensure that customer expectations and company interests are served while helping to promote MacDermid Enthone's exclusive line of products.

- Develop a business plan and sales strategy that ensures attainment of company sales and profit goals
- Prepare action plans for sales leads and prospects
- Initiate and coordinate action plans to penetrate new customers and markets
- Create and conduct proposal presentations and RFQ responses
- Possess the ability to calm a situation with customers, initiate a step-by-step plan, and involve other technical help quickly to find resolution

Hiring Profile

- Bachelor's Degree or 5-7 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Verifiable sales success in large complex sales situations
- Desire to work in a performance driven environment
- Excellent oral and written communication skills
- Decision making skills and the ability to multitask

apply now



Technology Communications Writer/Content Manager Board Systems Division

Mentor Graphics, a Siemens business, is a global technology leader in EDA software, enabling global companies to develop new and highly innovative electronic products in the increasingly complex world of chip, board, and system design.

Job Duties:

The Mentor printed circuit board (PCB) technical writer/content manager will:

- Write and produce high-quality content for various properties (blogs, product collateral, technical white papers, case studies, industry publications, etc.).
- Gather research and data, interview subject matter experts, and transform complex information into clear, concise marketing communications.
- Manage projects across multiple PCB product teams (high-speed design/analysis, advanced packaging, board design) within a deadline-driven environment.

Job Qualifications:

The ideal candidate should possess:

- Strong writing and editing skills with experience in PCB design technologies.
- Desktop publishing skills (InDesign) using project templates and knowledge of online publications and social media.
- A technical background (B.S. in electrical engineering or computer science preferred; this role works closely with the PCB division's technical marketing engineers and managers.
- Solid project planning and management skills; appreciation for adhering to deadlines; creativity for turning technical information into compelling content; teamwork and strong interpersonal communications skills; ability to be a self-starter.

apply now



PCB Equipment Sales

World-class manufacturer of wet process equipment for the PCB and plating industries, Integrated Process Systems Inc. (IPS) is seeking qualified candidates to fill a position in equipment sales. Potential candidates should have:

- Process engineering knowledge in PCB manufacturing
- Outside sales background
- Residency on the West Coast to manage West Coast sales
- Knowledge of wet process equipment
- Sales experience with capital equipment (preferred)

Compensation will include a base salary plus commission, dependent upon experience.

more details





Events Calendar

IPC High Reliability Forum for Mil-Aero and Automotive Sectors ►

May 15–17, 2018 Linthicum (Baltimore), Maryland, USA

Medical Electronics Symposium 2018 ►

May 16–18, 2018 Dallas, Texas, USA

IMPACT Washington, D.C. 2018 -

May 21–23, 2018 Washington, D.C., USA

2018 EIPC's 50 Years Anniversary Conference >

May 31–June 1, 2018 Bonn, Germany

JPCA Show 2018 >

June 6–8, 2018 Tokyo, Japan

IPC E-Textiles 2018 Workshop >

September 13, 2018 Des Plaines, Illinois, USA

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September 26–28, 2018 Bengaluru, India

electronicAsia 2018 >

October 13–16, 2018 Hong Kong

SMTA International >

October 16–17, 2018 Rosemont, Illinois, USA

TPCA Show 2018 ► October 24–26, 2018 Taipei, Taiwan

electronica 2018 ► November 13–16, 2018 Munich, Germany

HKPCA/IPC International Printed Circuit & South China Fair >

December 5–7, 2018 Shenzhen, China

Additional Event Calendars







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